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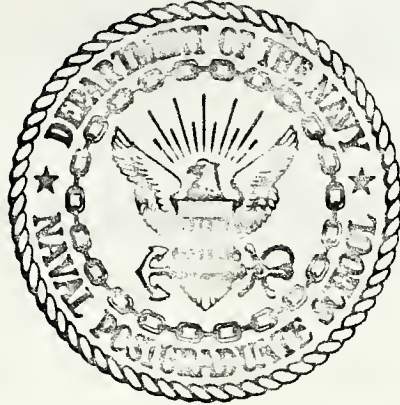
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A MICROPROGRAMMED I/O INTERFACE

Raimundo Nonato Daniel Duarte

NAVAL POSTGRADUATE SCHOOL

Monterey, California



THESIS

A MICROPROGRAMMED I/O INTERFACE

by

Raimundo Nonato Daniel Duarte

Thesis Advisor:

Raymond H. Brubaker

March 1974

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A MICROPROGRAMMED I/O INTERFACE

by

RAIMUNDO NONATO DANIEL DUARTE
LIEUTENANT - BRAZILIAN NAVY

Submitted in partial fulfillment of the
requirements for the degree of

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March 1974

ABSTRACT

This thesis presents a basic hardware model suitable for most sequential microprogrammed devices. A software system is described which allows the use of an assembly-level programming language instead of the binary representation of microcodes. The implementation of a microprogrammed input/output interface is presented as an example of use of both the hardware and software.

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I. INTRODUCTION

This thesis is part of a larger effort to implement a communications network for present and future computer systems at the Naval Postgraduate School. Microcomputers will be used in this network to replace as many interface hardware functions as possible with software, thus providing a degree of flexibility not attainable with hardware-only configurations. The need arose for a device which allows exchange of data and control signals between any of the computer systems and its associated microcomputer.

The aim of this thesis is to develop basic hardware that can be used in any of these interfaces, as well as in most sequential devices.

The IEM System/360 interface was chosen as the guide for design for the following reasons:

- a) it has a standard I/O interface between the data channel and the control units which activate I/O devices;
- b) it is possibly one of the more complex interfaces, thus providing a worst-case design.

During the course of work the need for a microprogramming language was recognized; the software designed to support it is described in chapter V.

II. IBM SYSTEM/360 I/O INTERFACE

A. OVERVIEW

Whenever the IBM System/360 channel wants to receive/send information from/to a specific I/O device it sends a command (Read/Write) to the device via its control unit and logically disconnects as soon as the control unit acknowledges the command. When the I/O device is ready to send/receive the desired information it signals to the channel which executes a polling sequence to find out which unit is asking for service. If the control unit is busy and cannot accept the command, a "Control Unit Busy Sequence" takes place, whereby the channel is notified and defers its request for a later point in time.

The control unit can also initiate a data exchange by signalling to the channel and waiting until it is ready to service the request.

Due to the number of signalling lines used, the detailed operational description is quite involved. It is described in Ref. 1. Reference 2 contains a somewhat more detailed and readable explanation of some of the different sequences.

B. INTERFACE FUNCTIONS

The rules which constitute the I/O Interface are physically implemented by 34 wires, or lines, whose state can be either up (one, high) or down (zero, low).

The lines are :

Bus Out - a set of nine lines used to transmit information (data, I/O device address, commands) from the channel to the control units. Eight lines are used to convey the information itself and one line is a parity bit. The type of information transmitted over Bus Out is indicated by the state of other lines.

Bus In - a set of nine lines used to transmit information (data, I/O device identification, status information) from the control unit to the channel. Eight lines are used to convey the information itself and one line is a parity bit. The type of information transmitted over Bus In is indicated by the state of other lines.

Address In (abbreviated AdrIn) - is a line from all attached control units to the channel. Its rise indicates that the address of the currently selected I/O device is available on BusIn .

Status In (abbreviated StaIn) - is a line from all attached control units to the channel. Its rise indicates that the control unit has placed status information on BusIn.

Service in (abbreviated SerIn) - is a line from all attached control units to the channel. Its rise indicates to the channel that the selected I/O device wants to transmit or receive a byte of information.

Command Out (abbreviated ComOut) - is a line from the channel to all attached control units. Its rise may indicate:

- 1) after the rise of AdrIn - the contents of BusOut is a command.

- 2) after the rise of SerIn - the channel is ending the current operation.

- 3) after the rise of StaIn - the control unit should disconnect from the interface after the fall of SelOut.

Service Out (abbreviated SerOut) - is a line from the channel to all attached control units. Its rise indicates to the selected I/O device that the channel has accepted the information on BusIn or has provided on BusOut the data requested by SerIn.

Suppress Out (abbreviated SupOut) - is a line from the channel to all attached control units and is used both alone and in conjunction with other outbound lines to provide the following special functions:

- 1) data suppression,
- 2) status suppression,
- 3) command chaining and
- 4) selective reset.

These functions are described in Ref. 1.

Operational Out (abbreviated OplOut) is a line from the channel to all attached control units and is used for interlocking purposes. Except for SupOut all lines from the channel are significant only when OplOut is up. Whenever OplOut is down, all inbound lines from the control units must drop and any operation currently in process must be reset.

Operational In (abbreviated OplIn) - is a line from all attached control units to the channel and is used to signal to the channel that an I/O device has been selected.

Select Out (abbreviated SelOut) - SelOut and SelIn form a closed loop from the channel through all attached control units and back to the channel.

Select In (abbreviated SelIn) - is the name given to SelOut when it reaches the channel after passing through all control units.

Hold Out (abbreviated HoldOut) - is a line from the channel to all attached control units and is used in conjunction with SelOut.

Address Out (abbreviated AdrOut) - is a line from the channel to all attached control units. It provides two functions:

1. I/O Device Selection - AdrOut up is an order to all attached control units to decode the I/O device address on BusOut.

2. Disconnect Operation - whenever HoldOut is down and AdrOut rises, or AdrOut is up and Hold Out falls, the presently connected control unit must drop OpIn, thus disconnecting from the interface.

Request In (abbreviated ReqIn) - is a line from all attached control units to the channel. Its rise indicates that a control unit is requesting a selection sequence.

Metering Out - is a line from the channel to all attached control units. Its rise indicates that the CPU meter is recording time.

Clock Out - is a line from the channel to all attached control units. Control units should not be allowed to switch from "On-line" to "Off-line" condition when ClcckOut is up.

The functions implied by the list above were to be implemented, resulting in the design of a device capable of acting as a control unit.

III. THE APPROACH

An interface to the /360 channel certainly had to include some logical circuitry. Preliminary studies showed that the state of the lines alone is not always sufficient to decide the action to be taken by the device. Therefore the nature of the functions to be performed was not strictly combinational, and the device would have to keep track of event sequences.

Another difficulty was that the number of variables involved, even reducing the problem to the bare essentials, was around seven; this implied the use of large reduction maps, difficult to visualize and error-inducing. The needed addition of flip-flop counters to make up for the sequential nature of some of the functions would aggravate the problem.

Furthermore, a troublesome and time-consuming implementation phase was anticipated for the design. If patchboards were to be used in the experimental implementation, poor contacts and misrouted wires were likely to compound with design errors; on the other hand, hardwired prototyping would be expensive if several corrections or changes were to be made.

These factors led to the use of microprogramming as opposed to hardwiring (or random logic).

IV. MICROPROGRAMMING

A. INTRODUCTION

Microprogramming, as used in this report, is a design technique substitute to hardwiring. The fundamental idea behind microprogramming is that, given a truth table with n inputs and one output, we can think of it as being a table of contents of a 2^n word, one bit per word, storage device.

The state of the inputs determines one unique address in the storage device and the content of this location is the desired value of the function.

It is easily seen that if, instead of one-bit words, the store had, say, eight-bit words, eight separate switching (binary) functions could be implemented. In the application described here, several binary function values are grouped into a field to specify one of several values. For example, a field of three bits can take eight different values. The same table can simultaneously implement several such functions.

The need was for a device capable of implementing the following basic flowchart operations:

- 1) Conditional branch - where the decision variable was to be one of the I/O interface lines.
- 2) Unconditional branch.

3) Execute predefined process - where the "predefined process" would be of the form "RAISE LINE..." or "DROP LINE..." only.

B. BASIC HARDWARE

Before introducing the complete model, its basic components will be presented and briefly explained.

1) Read Only Memory (ROM) (Figure 1) - depicted in the diagrams as a rectangle divided in three rows; the bottom row represents the input section and contains a description of the physical device as well as the input (address) bits. The middle row is subdivided in three fields :

leftmost field is the 'next basic address field' or ADR

center field is the 'select field' or SEL

rightmost field is the 'opcode field' or OPCODE

The upper row is subdivided in as many squares as the number of bits in each word of the ROM. The number inside the squares represent the significance of the bit (i.e. the binary order) .

7	6	5	4	3	2	1	0
ADR		SEL			OPCODE		
2	1	0					

Figure 1. An eight word, eight bits per word,
Read Only Memory.

2) Clock - depicted as the Greek letter phi(ϕ). Subscripts are used to differentiate among phases of the clock, i.e. ϕ_1 , ϕ_2 , ... ϕ_n are all pulse generators with the same frequency; however, the leading edge of the pulse which produces changes in the circuits under their control occurs at distinct time instants.

3) D flip-flops (Figure 2) - depicted as a square with the letter 'D' inside and subscripts whenever necessary to differentiate among the various flip-flops. Whenever the clock rises the output of the flip-flops becomes equal to the input value immediately prior to the clock pulse.

4) Data Selector / Multiplexer (MX) (Figure 2) - logic circuit with 2^n input lines, n select lines and one output line. It is the logical equivalent of a single-pole, 2^n -position switch whose position is specified by a n-bit input address. The output line presents the value of the single input-line selected by the select lines. In addition to the input and select lines, the multiplexer has a strobe or enable line. The output is valid only when the strobe line is zero (low).

5) Decoder / Demultiplexer (DMX) (Figure 2) - logic circuit with n inputs and 2^n outputs. For each binary value at the input, one different output line is dropped. In addition, the demultiplexer has a strobe or enable line. The selected output changes state only when the strobe line is low (zero).

C. OPERATION

The operation of the model is better explained by an example. The following assumptions are made:

- 1) The hardware configuration is as depicted in Figure 2.
- 2) The circuit is in steady-state operation.

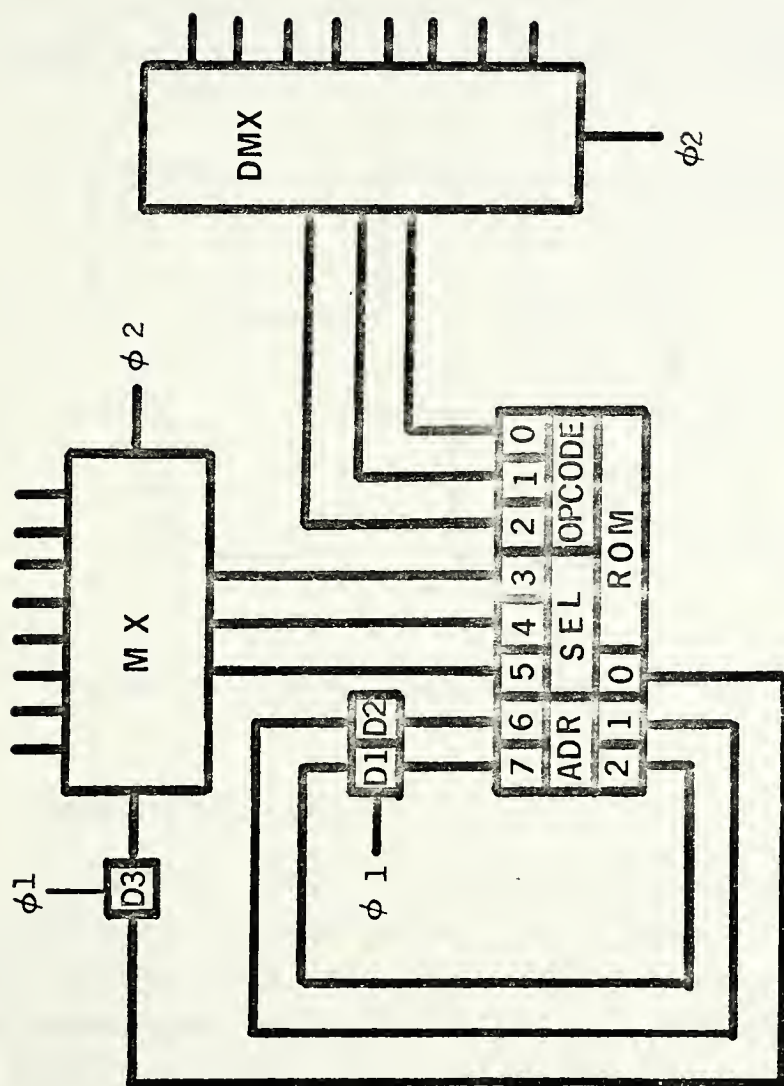


Figure 2. Basic hardware

3) The ROM has already been programmed and the contents of some addresses are tabulated below:

TABLE I			
ADDRESS	ADR FIELD	SEL FIELD	OPCODE FIELD
3	10	010	000
4	00	001	011
5	01	001	001
0	01	000	000
1	00	000	000

4) The two clocks ($\phi 1$ and $\phi 2$) run at, say, 500 KHz, their phase relationship being as shown in figure 3 .

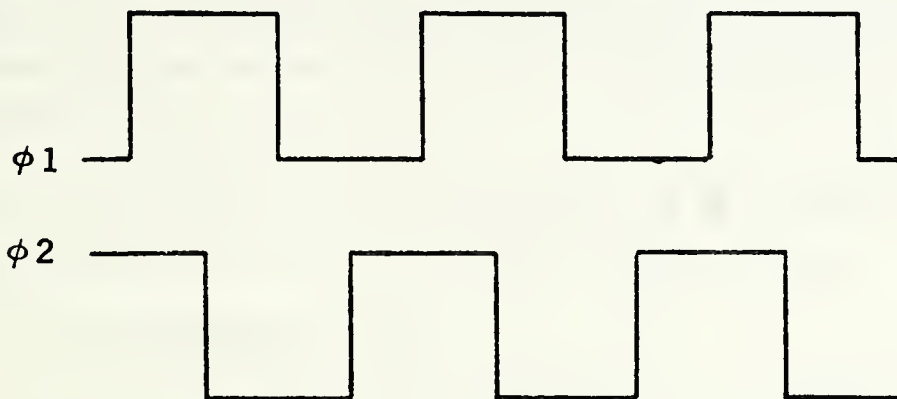


Figure 3. Phase relation between $\phi 1$ and $\phi 2$.

1. Conditional Jump

Refer to Table I and assume that the address now being accessed is number three. The inputs to D1 and D2 are 1 and 0 respectively (see "ADR FIELD") ; line two (010) has been selected (see "SEL FIELD") and the operation coded as 000 is being executed by some hardware external to the model (see "OPCODE FIELD"). Note that the outputs of D1, D2 and D3 must currently be 011 respectively, since we assumed ROM word three was being accessed.

Eventually the clock ($\phi 1$) will rise and the output of D1D2 will be 10, which implies that the address to be accessed is either 4 (100) or 5 (101) depending upon the output of D3. The output of D3 is the value of its input immediately prior to the $\phi 1$ pulse, and this is the value of input (to MX) line two (010); thus it cannot be said which ROM word will be accessed next without specifying the earlier state of this signal. The effect of this example can be described by the ALGOL-like statement:

"IF INPUT(2) GO TO 5 ELSE GO TO 4"

where input(2) is treated as a logical variable.

Soon after $\phi 1$, the outputs of the ROM start to change. Since it is not guaranteed that only one change in state will take place, $\phi 2$ is kept high at this point, thus preventing the output of DMX from being affected by this spurious input.

One microsecond later, $\phi 2$ goes low; consequently, the input of D3 is now defined and the right command is being enabled by one of the output lines of DMX.

2. Unconditional Jump

In the example described above, if it was known that input line two (010) had the value zero (it could be physically connected to ground), then the next address would have been forced to four. On the other hand, if it had the value 1 (connected to the power supply), an unconditional jump to location five would have resulted.

Therefore, to implement the unconditional jump, it suffices to save two input lines to MX and set them to 1 and 0 respectively.

3. Execution of a Predefined Process

It can be seen from the two previous examples that the output of DMX depends upon the particular address being accessed. By proper selection of the contents of the "next address" field, it is therefore possible to make the ROM

cause the execution of sequences of processes, as will be described.

Assuming that this hardware was to be used as control unit for an Arithmetic and Logic Unit of a computer, certain basic functions would be needed, such as adder, multiplier, divider, comparator, etc. These basic functions are collectively called "microspec functions" by Husson (Ref. 2). The microspec function has one enable line that activates it.

The hardware in the example allowed coding of eight possible operations. Therefore, if the output lines of DMX were connected to suitable microspec functions, up to eight different predefined processes could be selected and executed.

V. ALMIC - AN ASSEMBLY - LEVEL LANGUAGE FOR MICROPROGRAMMING

A. MOTIVATION

Given the basic hardware model described in chapter IV, the next task was the actual programming of the RCM's to generate the control sequences required by the /360 channel. This meant:

- 1) find the bit patterns to be stored in each field of each address;
- 2) put them on paper;
- 3) actually write them into the ROM.

The last operation was relatively easy, because all that is required is equipment already available. However, the first two proved not only tedious but also highly error-prone. In the case under study it was estimated that a 256 word, 16 bits per word, store would be needed, which implied a sizable number of bit strings to be input via a teletypewriter. In case an error was detected, or a change sought, most of the work would have to be done again.

It was decided that a higher level language would be desirable to allow straightforward description of control sequences and to automate their translation into ROM bit patterns. This required the design of a software package to support it and, due to time constraints, it was agreed that an assembler-level language would be more reasonable and still helpful.

The general format of a statement in the assembler language is given by the example:

34 : 28 , ADROUT,STAIN.

where the number before the colon (34) is the address where the statement is to be stored; the first field (28) is the next address (not the "next basic address" mentioned in chapter IV; the assembler will take care of this detail); ADROUT, in the example, stands for "select the decision line ADROUT" and the third field is the operation to be performed, "raise line StaIn (Status In)" in this case.

It is to be understood by this example that the next instruction will be in the address given by:

$\{28 + (\text{current value of ADROUT, 1 or 0})\}$
therefore 28 or 29.

B. THE SOFTWARE PACKAGE

1. Introduction

The model presented in chapter IV was intended to be used in any sequential microprogrammed circuit. Therefore, before attempting to write programs for any specific hardware configuration, it is necessary to furnish the assembler with the following information:

- 1) number of addresses in the ROM;
- 2) number of bits in each field of a ROM word;
- 3) list of mnemonics used to represent the input lines to MX;
- 4) list of mnemonics used to represent the opcodes (or microspec functions).

2. Functional Description and Use of the Software Package

The package is composed of three main programs:

- a) the DATA GENERATOR
- b) the TABLE GENERATOR
- c) the ASSEMBLER

In addition there are 13 subroutines: INIT, GNC, CONV, GET, PUT, ICON, PAD, ERROR, WRITEL, FORM, CCNCUT, SCAN, PUNCH.

a. The Data Generator

(1) Purpose. Generate input data for the Table Generator.

(2) Input. Input is in free-format 80-column records, with different elements separated by commas, except where otherwise noted. Blanks are always irrelevant, therefore "2 5 6 , 34." is the same as "256,3 4.". The following data is required:

(a) one card with the number one in column one;

(b) the number of fields in a ROM word, followed by a comma. This is necessary since it is allowed to separate the opcode field into as many sub-fields as wanted, thus providing the capacity to execute several operations simultaneously;

(c) the number of bits in each field of the ROM word;

(d) list of mnemonics used to represent the input lines to MX. The last mnemonic is to be followed by a period, not a comma;

(e) list of mnemonics used to represent the microspec functions. The last mnemonic (in each sub-field, if more than one is used) is to be followed by a period, not a comma.

(3) Output. The output is in form of punched cards ready to be fed to the Table Generator.

b. The Table Generator

(1) Purpose. Sets up tables to be used by the Assembler.

(2) Input. Input is in free-format 80-column records, with different elements separated by commas, except where otherwise noted. Blanks are always irrelevant. The following data is required :

(a) one card with the number two in column one;

(b) number of fields in each RCM word, followed by a comma;

(c) number of bits in each field, followed by a comma;

(d) list of mnemonics used to represent the input lines to MX. Each mnemonic is to be followed (after a comma) by its corresponding binary code;

(e) list of mnemonics used to represent the microspec functions, each mnemonic being followed (after a comma) by its corresponding binary code.

(3) Output. Fortran DATA statements ready to be inserted into the "Block Data" subprogram for use with the Assembler.

c. The Assembler

(1) Purpose. Converts statements of the form:
<label> : <address>,<select line>,<opcode>.

for example: 25 : 36 , SELOUT, DPSELOUT.
into bit patterns suitable to program a ROM.

(2) Input. The first card must have the number three in column one. For the program itself, input is in free-format 80-column records. Comments can be interspersed with (and even within) statements, provided

they are enclosed between the signs "<" and ">" . The card after the last in the program being assembled must have a "*" in column one.

(3) Output. Paper tape in a format suitable to program a ROM.

VI. IMPLEMENTATION OF A MICROPROGRAMMED INTERFACE

This section is composed of two parts; part A contains a description of the procedure used to implement the interface. In part B an example is given to illustrate and clarify the procedure described in part A.

A. OVERVIEW

The following steps should be adopted in designing a microprogrammed device using the hardware and software presented in chapters IV and V :

Step 1. Make a flowchart representation of the behavior of the device. This flowchart is to use the "binary decision" and the "predefined process" boxes only.

Step 2. Count the number of distinct decision variables. Call it m .

Step 3. Count the number of distinct predefined processes. Call it n .

Step 4. Count the number of decision boxes. Call it p .

Step 5. Determine the number of fields (not bits) to be used in microprogramming the ROM. The least number is three, and will be greater if and only if more than one microspec function has to be activated at the same time.

Step 6. Determine the number of bits in each field. For the "next basic address" field it will be:

$$[\log_2 2p] - 1$$

where $[x]$ means the least integer not less than x .
For the "select field" the number of bits will be:

$$a = \lceil \log_2 m \rceil$$

For the "cpcode field" it will be $\lceil \log_2 n \rceil$.

Step 7. Choose the component to play the role of MX. It will be a Data Selector/Multiplexer with at least "a" input bits.

Step 8. Choose the component to play the role of DMX. It will be a Decoder/Demultiplexer of capacity at least n to n^2 .

Step 9. Design the hardware necessary to implement the microspec functions according to the specific needs of the project.

Step 10. Run the Data Generator using as inputs:

- a) number of fields in each ROM word, followed by a comma;
- b) number of bits in each field of the ROM, each followed by a comma;
- c) list of mnemonics used to represent the input lines to MX. Each mnemonic is to be followed by a comma, except the last one, which shall be followed by a period;
- d) list of mnemonics used to represent the microspec functions. Each mnemonic is to be followed by a comma, except the last one, which shall be followed by a period.

Step 11. Run the Table Generator using the output of the Data Generator as its input.

Step 12. Insert the output of the Table Generator in proper place within the "Block Data" subprogram for use with the Assembler.

Step 13. Using the algorithm presented in Appendix B, label the boxes of the flowchart.

Step 14. Using the algorithm presented in Appendix C, write the microprogram and punch it.

Step 15. Run the Assembler using the microprogram as input. The program is currently written in FORTRAN for a XDS-9300 computer. To run the Assembler in other computers minor changes are necessary. As examples, the compiler may not accept more than 20 continuation cards which requires breaking up the "DATA MEMORY" statement inside the "Block Data" subprogram into smaller statements; the logical number for the output unit (paper tape punch) was assumed to be seven.

The output of the Assembler is a paper tape ready to be fed to the MCS-8 PROM Programming System.

B. EXAMPLE

The I/O Interface for the System/360 will be used to demonstrate the method just described. Figures 4 and 5 contain a block diagram of the complete circuit.

From Figure 4 it can be seen that inputs to MX number 0 and 1 were reserved to implement unconditional jumps. Inputs two thru six are outbound tags from the channel. Input seven will be provided by the associated microcomputer, having the value of one whenever the microcomputer, or the device attached to it, is busy. Inputs nine and ten are provided by the hardware shown in Figure 5. Input ten is tapped from the Status In line.

Figure 5 displays the executive part of the interface hardware. Output line number zero for the DMX was reserved to represent "no operation" to be performed. Lines one and two respectively raise and drop the "channel-initiated-sequence" line which is fed to MX in Figure 4. The squares with the letters R and D are latches whose outputs switch to 1 when R (raise) is zero and to zero when D (drop) is zero.

Output lines three and four implement the SelOut control. Lines five thru 13 control the multiplexing of

data, status and address into BusIn. At the same time, lines six and seven, nine and ten and 12 and 13 implement SerIn, AdrIn and StaIn respectively.

Whenever the microcomputer wants to send/receive information to/from the channel, it will raise ReqIn, which will be dropped by output line 16.

In the sample design which follows the "reset" and the "disconnect" sequences (described respectively under "Operational Out" and "Address Out" in chapter II) were not considered. The action to be taken in case of wrong parity on the address byte was also omitted.

Step 1. The flowchart will be as shown in Appendix A.

Step 2. The decision variables are: 0, 1, ADROUT, SELOUT, SUPCUT, COMOUT, SEROUT, CUBUSY, CHSEQ, OURADR, STAIN; therefore $m = 11$.

Step 3. The predefined processes are :NO OP, CHSEQ, DCHSEQ, PSELOUT, DPSELOUT, DATABUSIN, DSERIN, SERIN, STABUSIN, DSTAIN, STAIN, ADRBUSIN, DADRIN, ADRIN, CPLIN, DCPLIN, LREQIN, TSTADR. Therefore $n = 18$.

Step 4. There are 20 decision boxes, thus $p = 20$.

Step 5. Three fields only will be used, as there is no need for simultaneous execution of microspec functions.

Step 6. Number of bits in "next basic address field":

$$[\log_2 2 \times 20] - 1 = 5$$

number of bits in "select field": $a = [\log_2 11] = 4$

number of bits in "opcode field": $[\log_2 18] = 5$

The size of ROM address space will be the number of possible "next basic addresses", $2^5 = 32$, doubled (for the two different states of the address bit from D6, Figure 4); a total of 64 words in this case. Each word shall have at least 14 bits. Intel's 1702A has 256 words, eight bits per word, and is reprogrammable. Connecting two of them as in figure 6 a 256 word, 16 bits per word, store is obtained.

Step 7. MX will have four inputs; Signetics N74150 is suitable.

Step 8. DMX has 32 outputs; since no decoder is available with so many outputs, two Signetics N74154's will be used, connected as in Figure 7. Bit 0 of ROM will act as "chip selector".

Step 9. There are eight microspec functions of the form: "Raise/Drop line...", namely, CHSEQ/DCHSEQ, PSELOUT/DPSELOUT, STAIN/DSTAIN, SERIN/DSERIN, ADRIN/DADRIN, OPLIN/DOPLIN, DREQIN, TSTADR.

The logic circuit to perform this operation will have two inputs (Raise and Drop, or R and D) and one output. The inputs should be level-triggered by the low signal, as this is the output available from DMX. Therefore, the corresponding truth table is as depicted in Figure 8a; Figure 8b shows one possible implementation.

For the three functions which deal with BusIn (DATABUSIN, STABUSIN, ADREUSIN) a set of eight AND-OR gates working as a multiplexer will suffice. The data and status bytes will be provided by the microcomputer, while the address byte will come directly from BusOut.

The address of an I/O device can be any eight-bit pattern. The address checking function (TSTADR) will have eight inputs, to be fed by BusOut. It is necessary to have some switching capability in order to select, at installation time, the range for valid addresses. The output is one line (OURADR), which will have the value one whenever the input address is within range. Figure 9 shows the logical circuit to perform the function. The switch S will be in position one for those bits which must be one for the address to be accepted, in position two for those bits which must be zero, and in position three for those bits which are irrelevant.

Step 10. The input to the Data Generator is displayed in Figure 10a, whereas part b of the same figure shows the output obtained.

Step 11. The output of the Table Generator is displayed in Figure 11.

Step 12. The output of the Table Generator is inserted in the "Block Data" subprogram.

Step 13. The flowchart of Appendix A was numbered using the algorithm described in the previous section.

Step 14. The resulting microprogram is listed in Figure 12.

Step 15. Using the input shown in Figure 12 to run the Assembler, the output will be a paper tape ready to microprogram the RCM.

VII. CONCLUSION

This thesis dealt with the design of a microprogrammed I/O interface to be used in a communications network at the Naval Postgraduate School.

A basic hardware approach suitable to most microprogrammed sequential applications was described along with an assembler-level language for microprogramming.

The fact that it was possible to devise an algorithm to write the AIMIC microprogram suggests that it might be feasible to improve the software package to the point where the flowchart itself, and not the program, would be used as input to the system; the flowchart, as used here, can be represented by some sort of binary tree.

In order to implement and test the interface it is necessary to incorporate in this design the hardware and also the microinstructions needed to handle the exchange of information between the device and the microcomputer.

APPENDIX A

This appendix contains the flowchart used to implement the I/O interface between the System/360 channel and the device described in this thesis. It was obtained from Appendix C of Ref. 1 by eliminating all boxes "under responsibility of the channel" and by adding others necessary to specify operations to be performed by the device.

As to the mnemonics used, the following general rules apply:

a) the name of a line inside a decision box means: "Is the line up?";

b) the name of a line inside a process box means: "Raise line";

c) the name of a line inside a process box when preceded by the letter "D" means "Drop line".

The lines are :

ADRBUSIN-Address byte to BusIn

ADRIN-Address In

ADROUT - Address Out

CHSEQ- Channel-Initiated-Sequence

COMOUT - Command Out

DATAEUSIN-Data byte to Bus In

OPLIN-Operational In

PSELCUT - Propagate Select Out

REQIN-Request In

SELOUT -Select Out

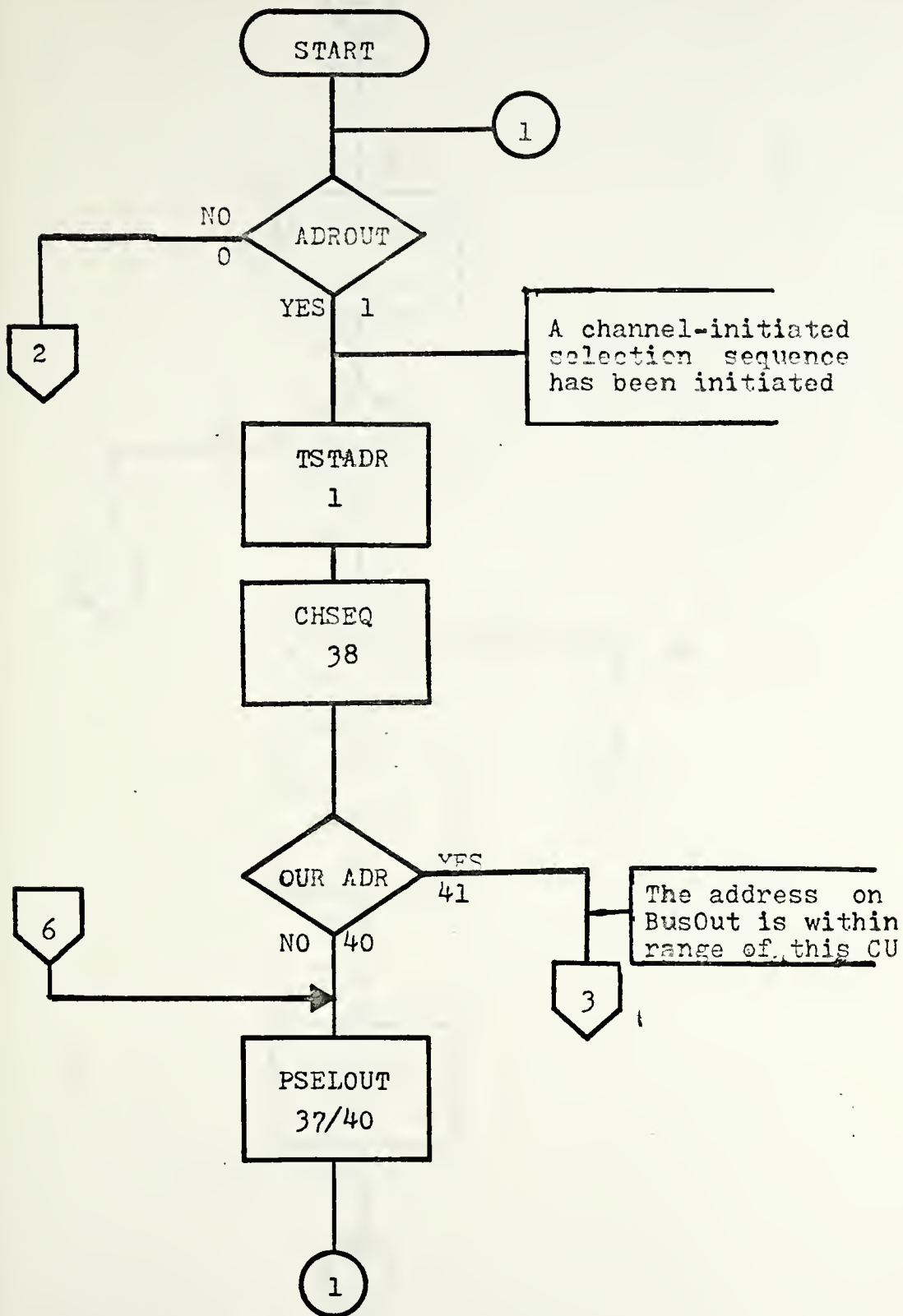
SERIN-Service In

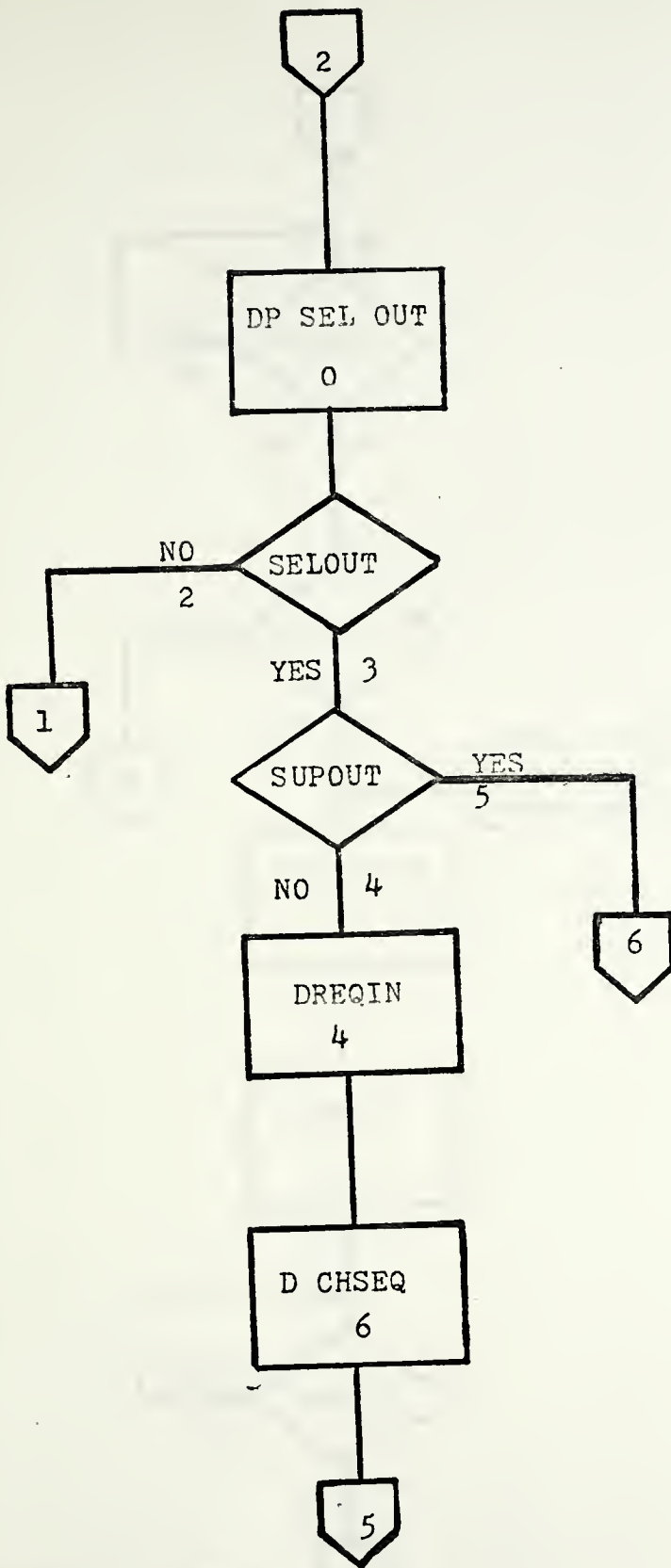
SEROUT - Service Out

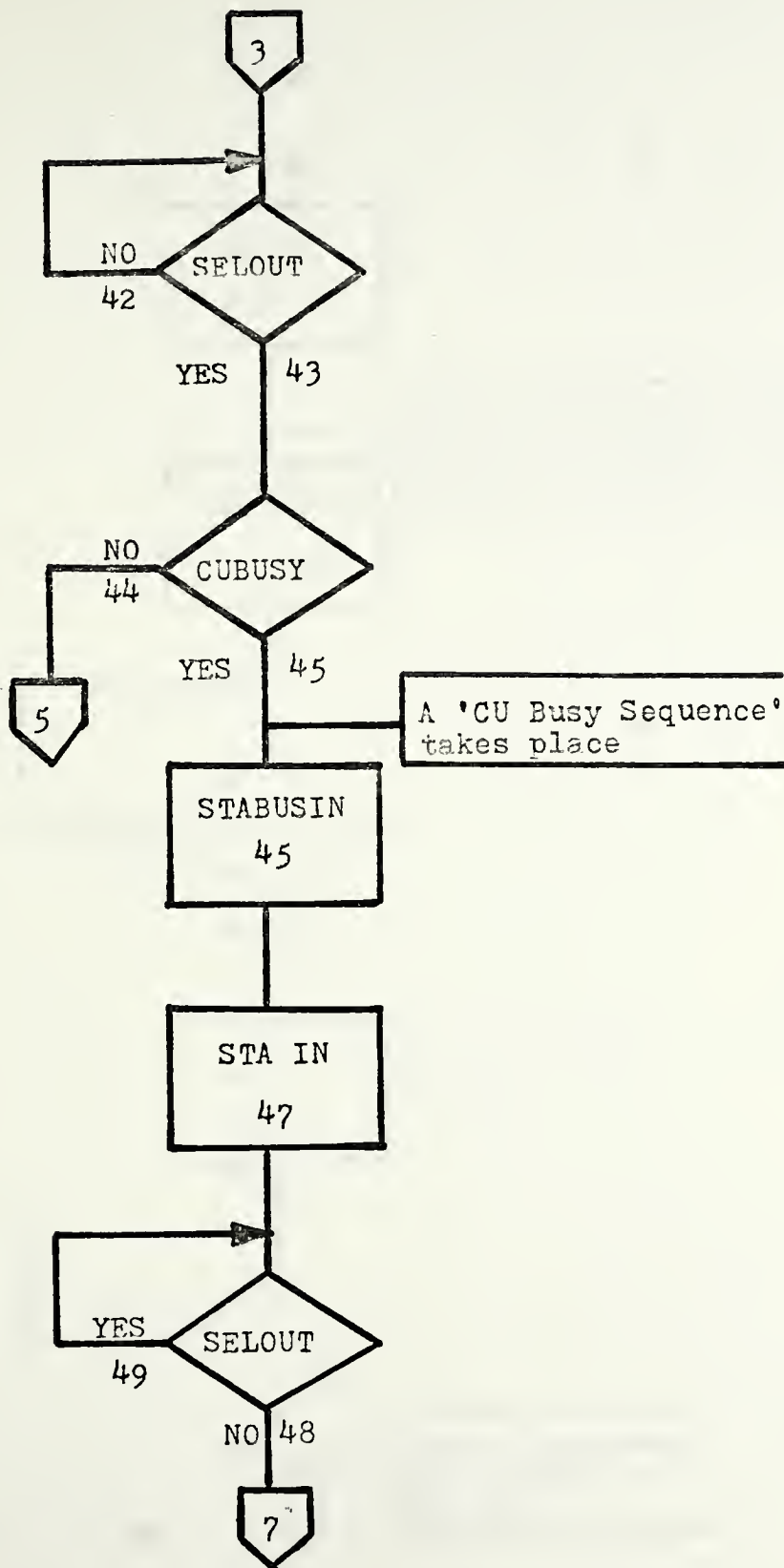
STABUSIN-Status byte to BusIn

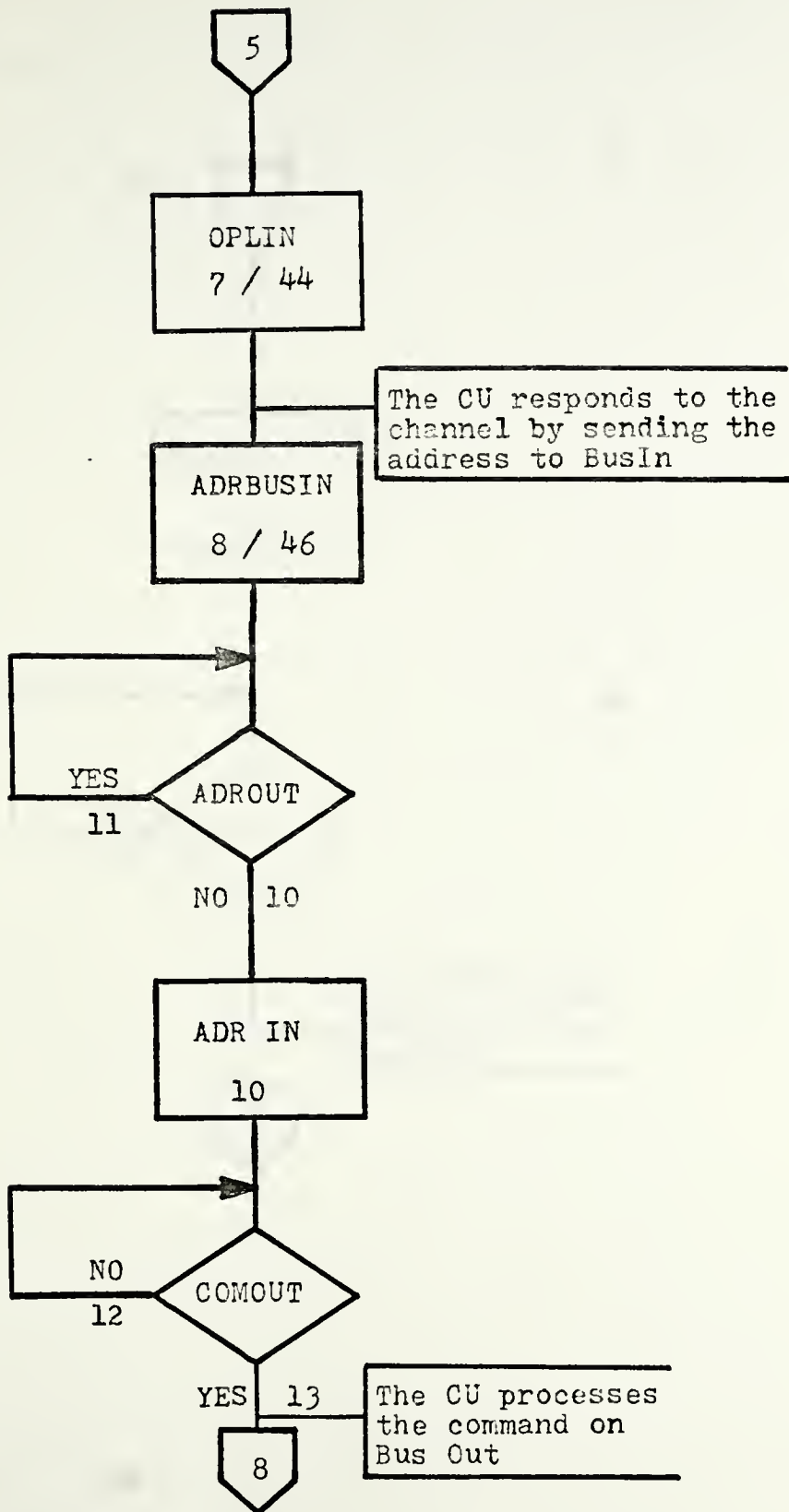
STAIN-Status In

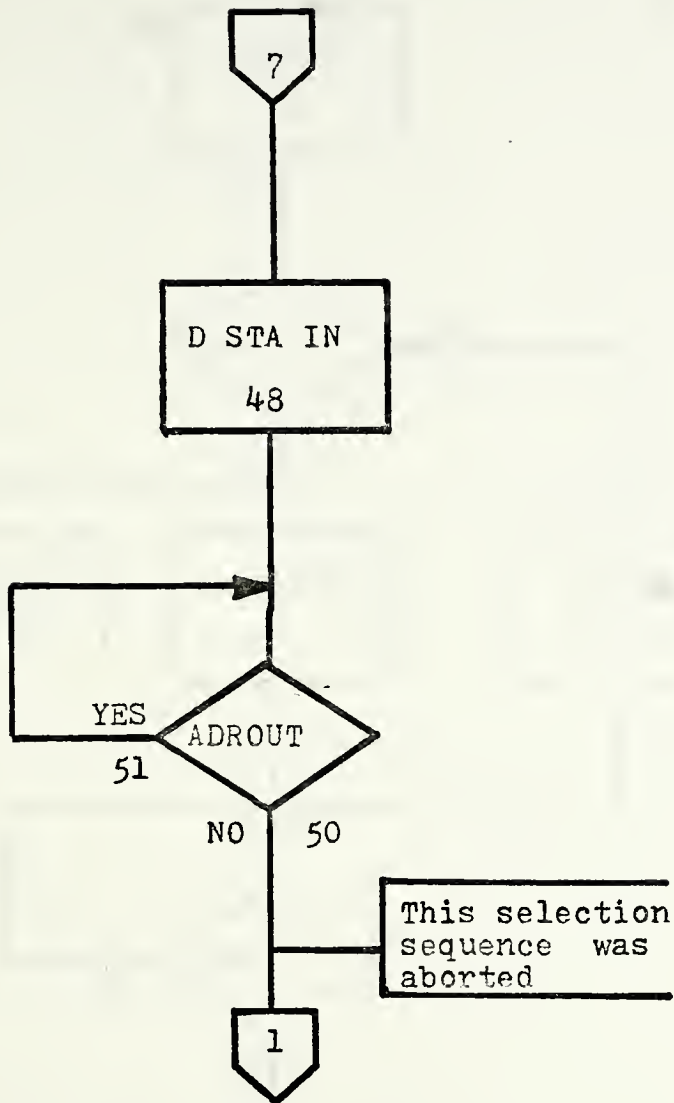
SUPOUT - Suppress Out

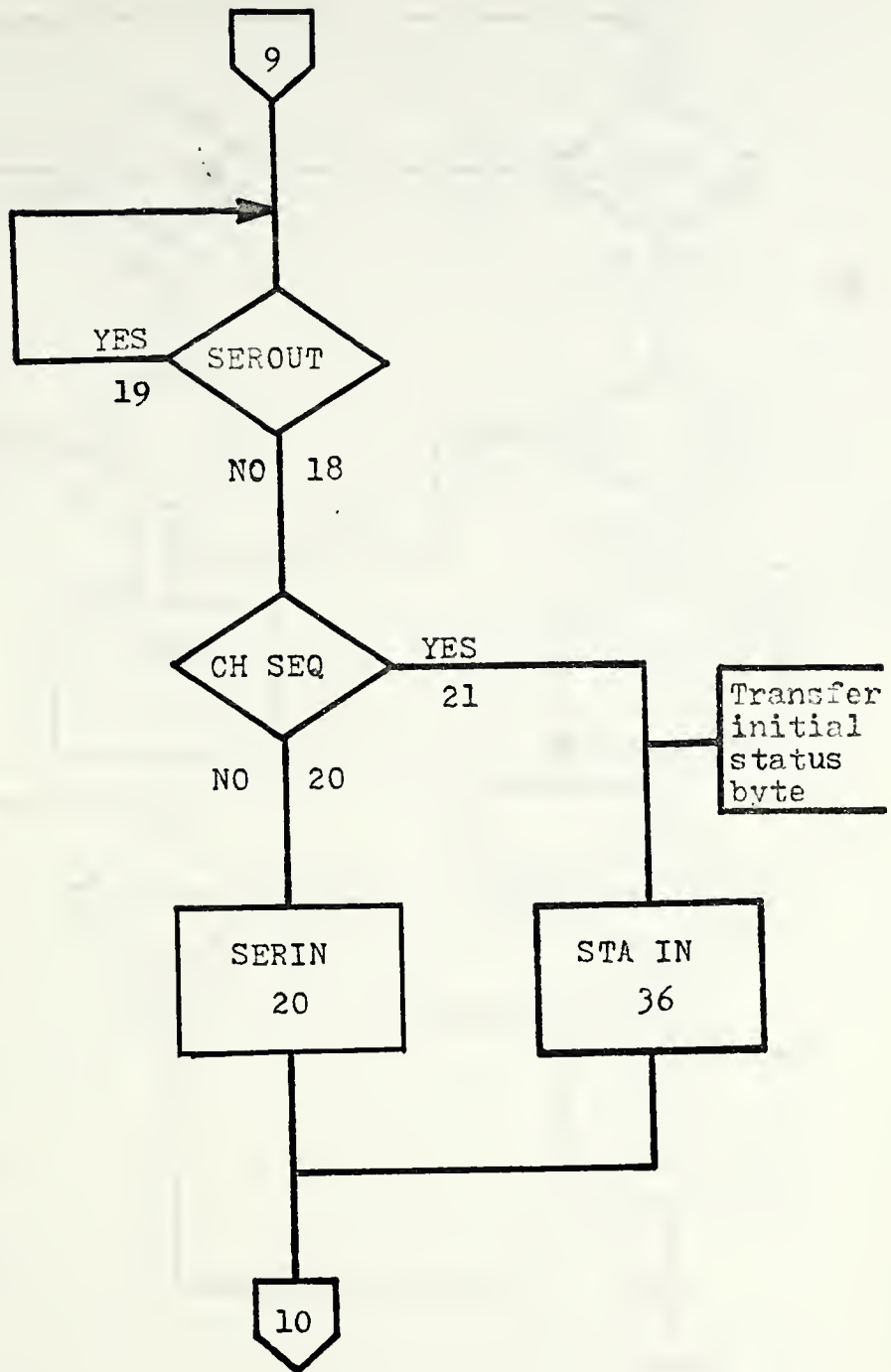


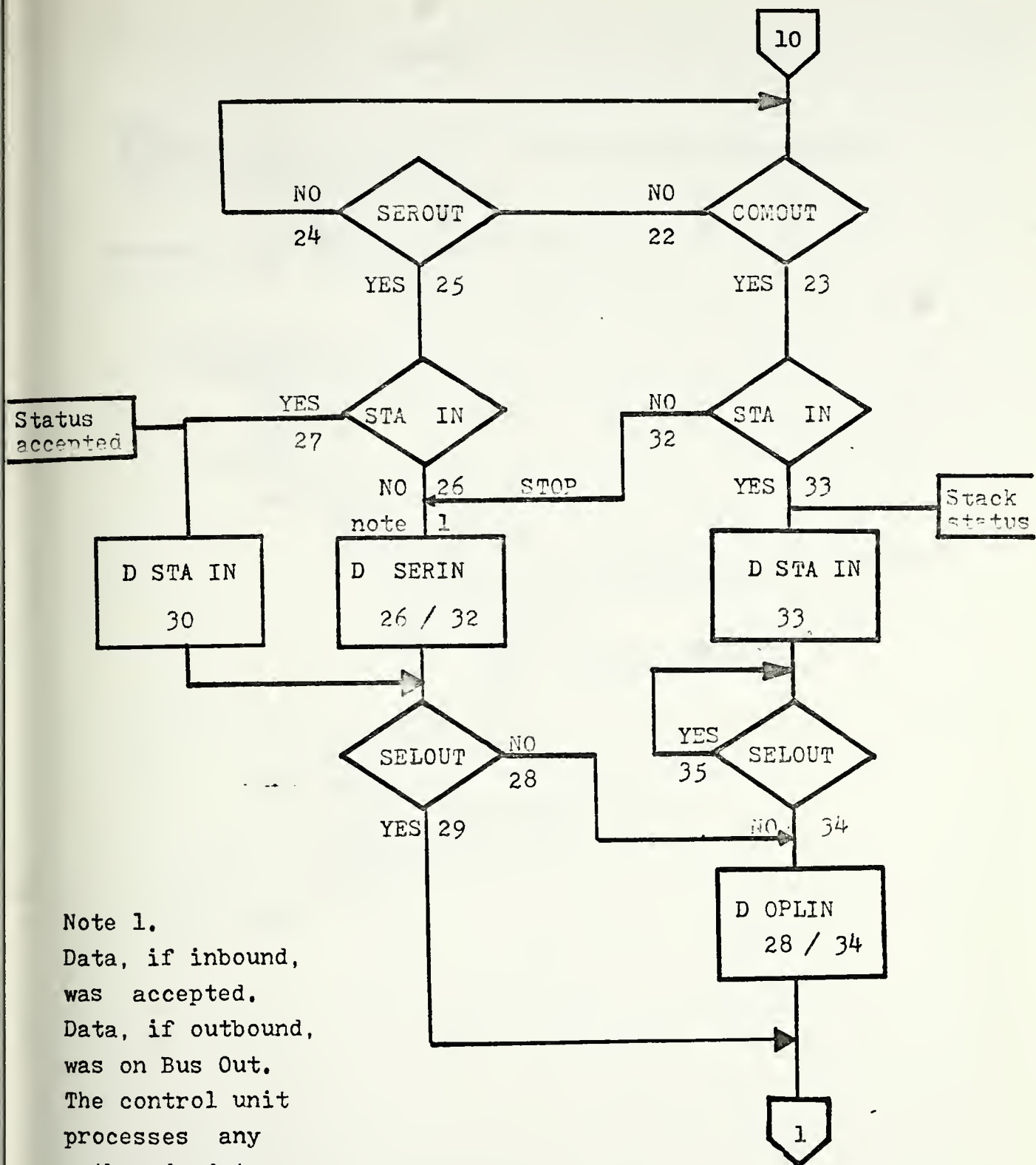












APPENDIX B

```

BEGIN
INTEGER I ;
RECORD POINTER(INTEGER LAST; REFERENCE(POINTER)NEXT);
REFERENCE(POINTER) TOP;

COMMENT : SET YOURSELF AT 'START' BOX ;
I := 0 ; TOP := NULL ;

A : TAKE NEXT BOX ;
    IF RECTANGULAR
    THEN BEGIN
        LABEL IT WITH I ;
        I := I + 1 ;
        GO TO A
    END
    ELSE BEGIN
        IF ALREADY VISITED
        THEN BEGIN
            IF TOP = NULL
            THEN GO TO STOP
            ELSE BEGIN
                COMMENT : SET YOURSELF AT 'YES' BRANCH
                CORRESPONDING TO LAST(TOP);
                TAKE NEXT BOX ;
                IF RECTANGULAR
                THEN BEGIN
                    LABEL IT WITH LAST(TOP) ;
                    TOP := NEXT(TOP) ;
                    GO TO A
                END
                ELSE GO TO C
            END
        END
    ELSE BEGIN
        IF I IS ODD THEN I := I + 1 ;
        LABEL 'NO' BRANCH WITH I ;
        LABEL 'YES' BRANCH WITH I + 1 ;
        I := I + 2 ;
        GO TO B
    END
END;

```



```

B : TOP := POINTER (LABEL OF 'YES' BRANCH, TOP) ;
   TAKE BOX CONNECTED TO 'NO' BRANCH ;
   IF RECTANGULAR
   THEN BEGIN
        LABEL IT WITH I - 2 ;
        GO TO A
      END
   ELSE BEGIN
        IF ALREADY VISITED
        THEN BEGIN
              IF TOP = NULL
              THEN GO TO STOP
              ELSE BEGIN
                    COMMENT : SET YOURSELF AT 'YES'
                    BRANCH CORRESPONDING TO LAST(TCP) ;
                    TAKE NEXT BOX;
                    IF RECTANGULAR
                    THEN BEGIN
                          LABEL IT WITH LAST(TOP) ;
                          TOP := NEXT(TOP) ;
                          GO TO A
                        END
                    ELSE GO TO C
                  END
              END
        ELSE BEGIN
              IF I IS ODD THEN I := I + 1 ;
              LABEL 'NO' BRANCH WITH I ;
              LABEL 'YES' BRANCH WITH I + 1 ;
              I := I + 2 ;
              GO TO B
            END
        END ;
END ;

C : TOP := NEXT(TOP) ;
   IF ALREADY VISITED
   THEN BEGIN
        COMMENT : SET YOURSELF AT 'YES'
        BRANCH CORRESPONDING TO LAST(TCP) ;
        TOP := NEXT(TOP);
        GO TO A
      END;
   IF I IS ODD THEN I := I + 1 ;
   LABEL 'NO' BRANCH WITH I ;
   LABEL 'YES' BRANCH WITH I + 1 ;
   I := I + 2 ;
   GO TO B ;
STOP : END.

```


APPENDIX C

In order to write an ALMIC statement, all that is needed is to write the address number followed by a colon and then:

a) for the "next address" field:

1) find the label in the flowchart corresponding to the desired address;

2) the next address is the label of the next box if it is a process box or the label of the "no" branch otherwise.

b) for the "select" field :

1) find the label in the flowchart corresponding to the desired address;

2) if the next box is a decision box, use its contents as "select" field;

3) if the next box is an even numbered process box, use zero; otherwise use 1 for "select" field.

c) for the "opcode" field :

1) find the label in the flowchart corresponding to the desired address.

2) if it belongs to a process box use its contents as "opcode" ; otherwise leave blank.

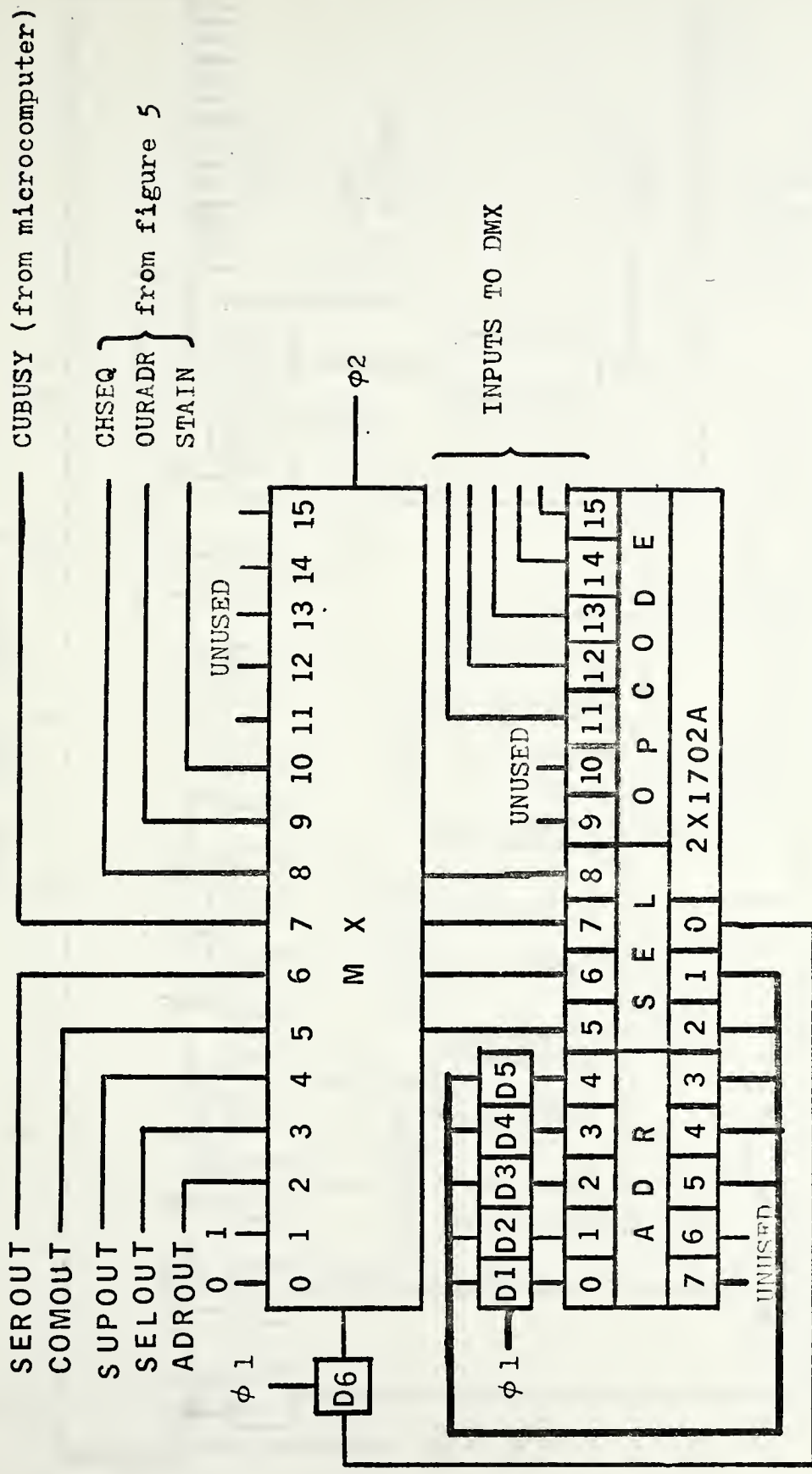


Figure 4. Control portion of the interface

INPUT FROM FIGURE 4

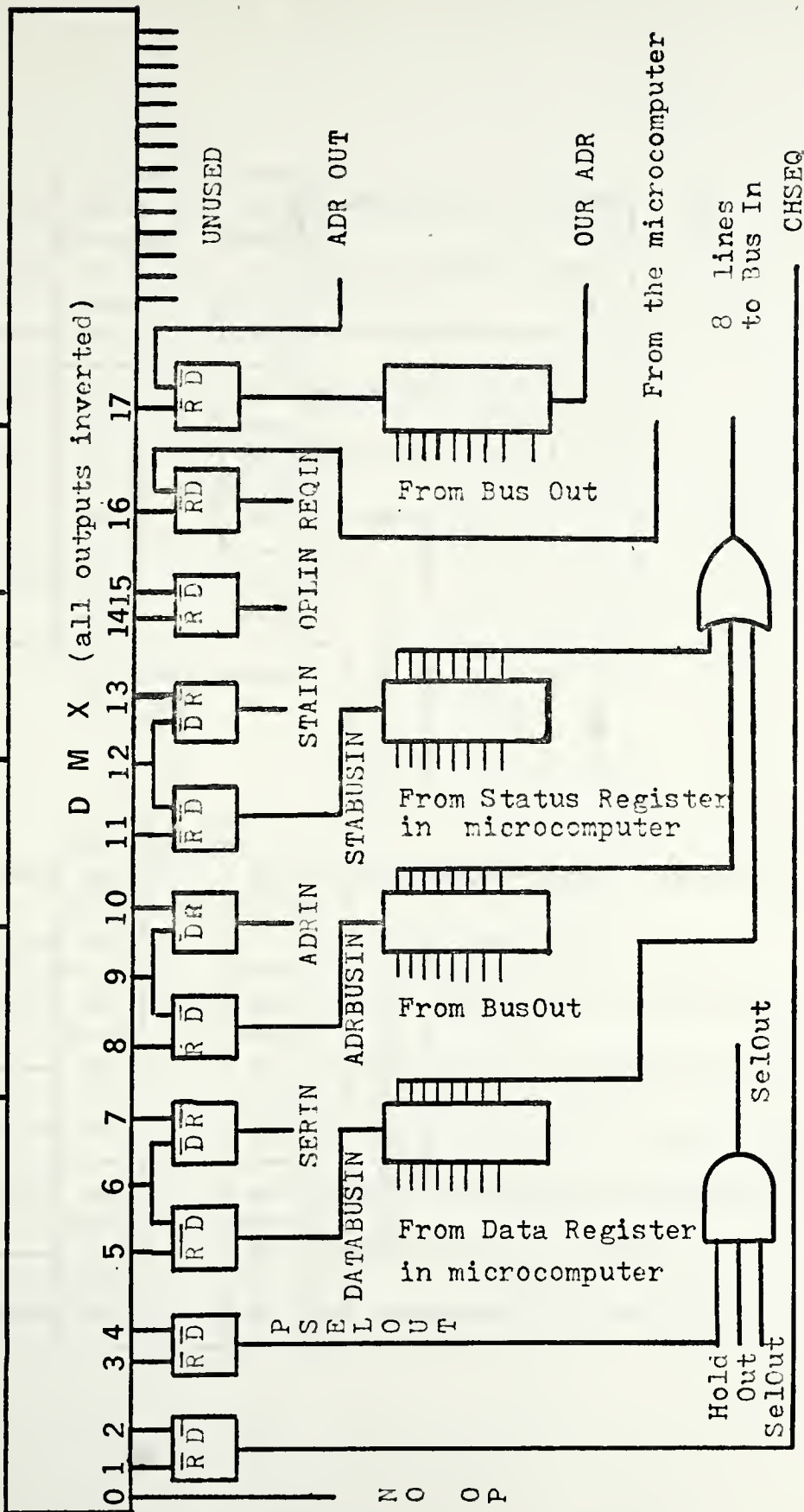
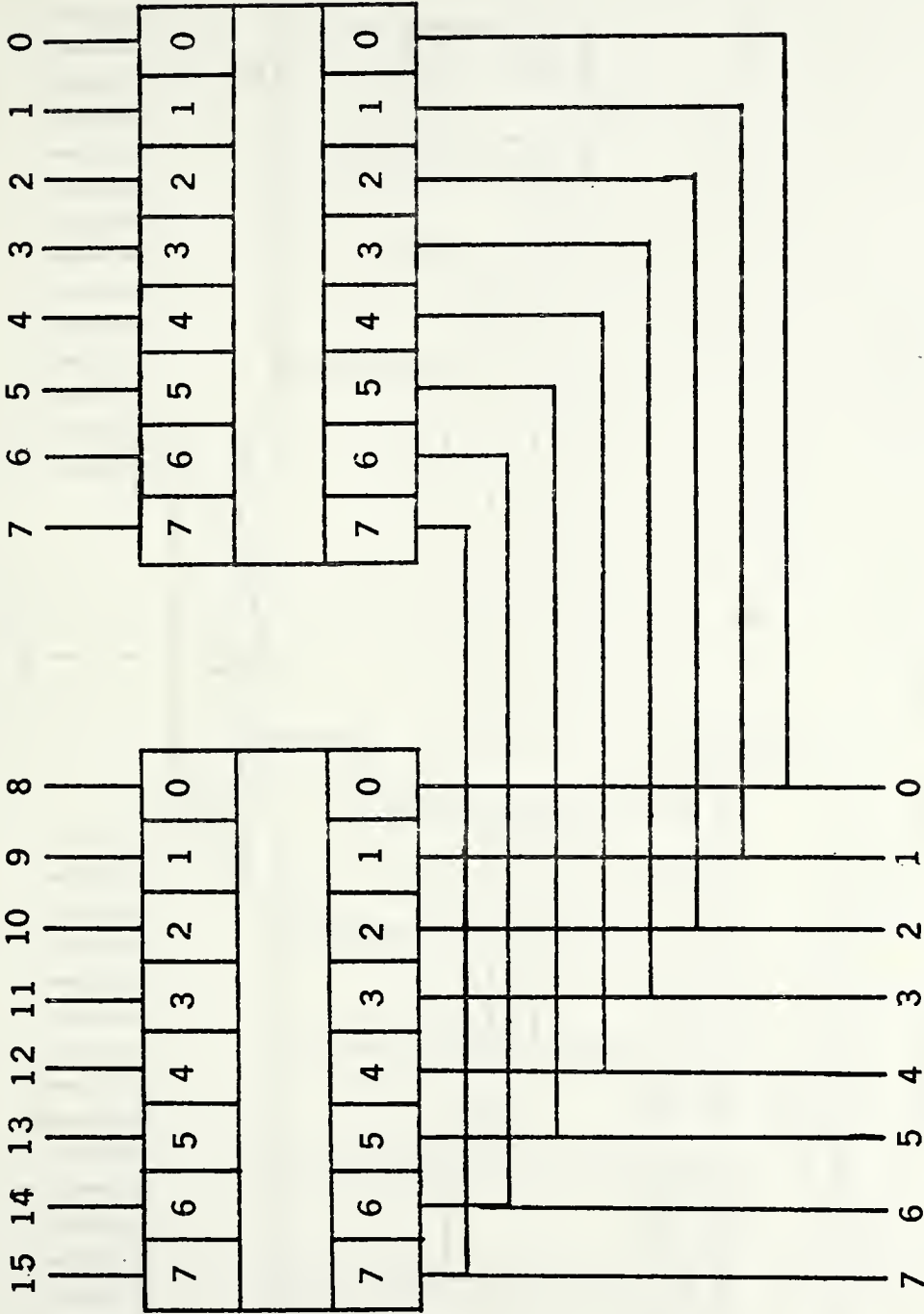


Figure 5. Executive part of the interface

OUTPUT BITS



INPUT BITS

Figure 6. Parallel connection of two ROMs

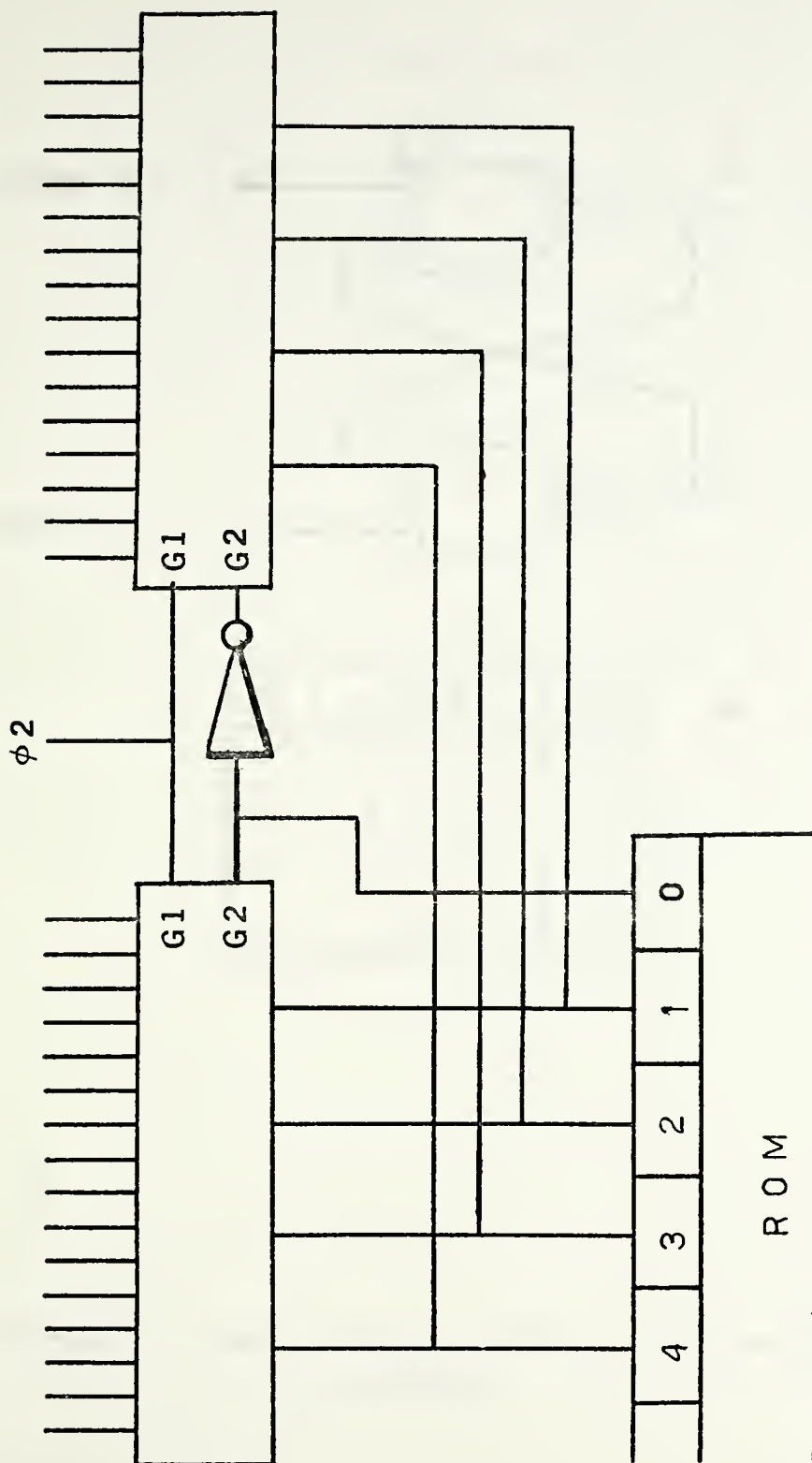
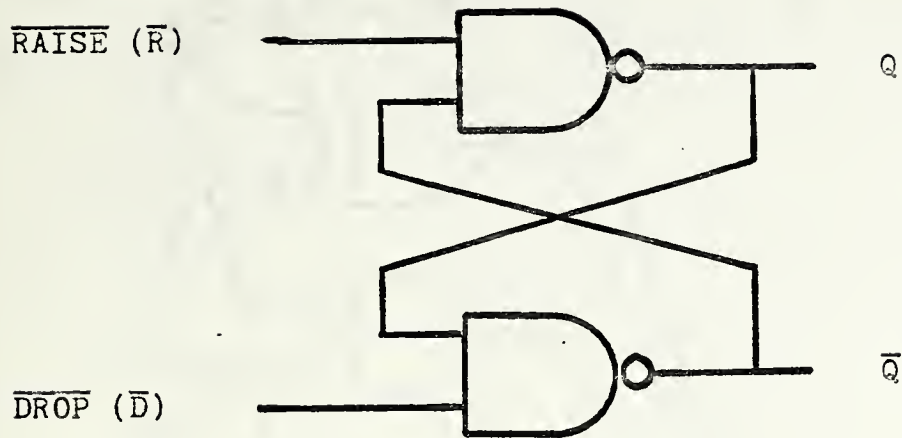


Figure 7. Parallel connection of Decoders



(b)

\bar{R}	\bar{D}	Q	\bar{Q}	Q^+	\bar{Q}^+
0	0	X	X	X	X
0	1	X	X	1	0
1	0	X	X	0	1
1	1	X	X	Q	\bar{Q}

(a)

Figure 8. Latch circuit for the Raise/Drop Line function

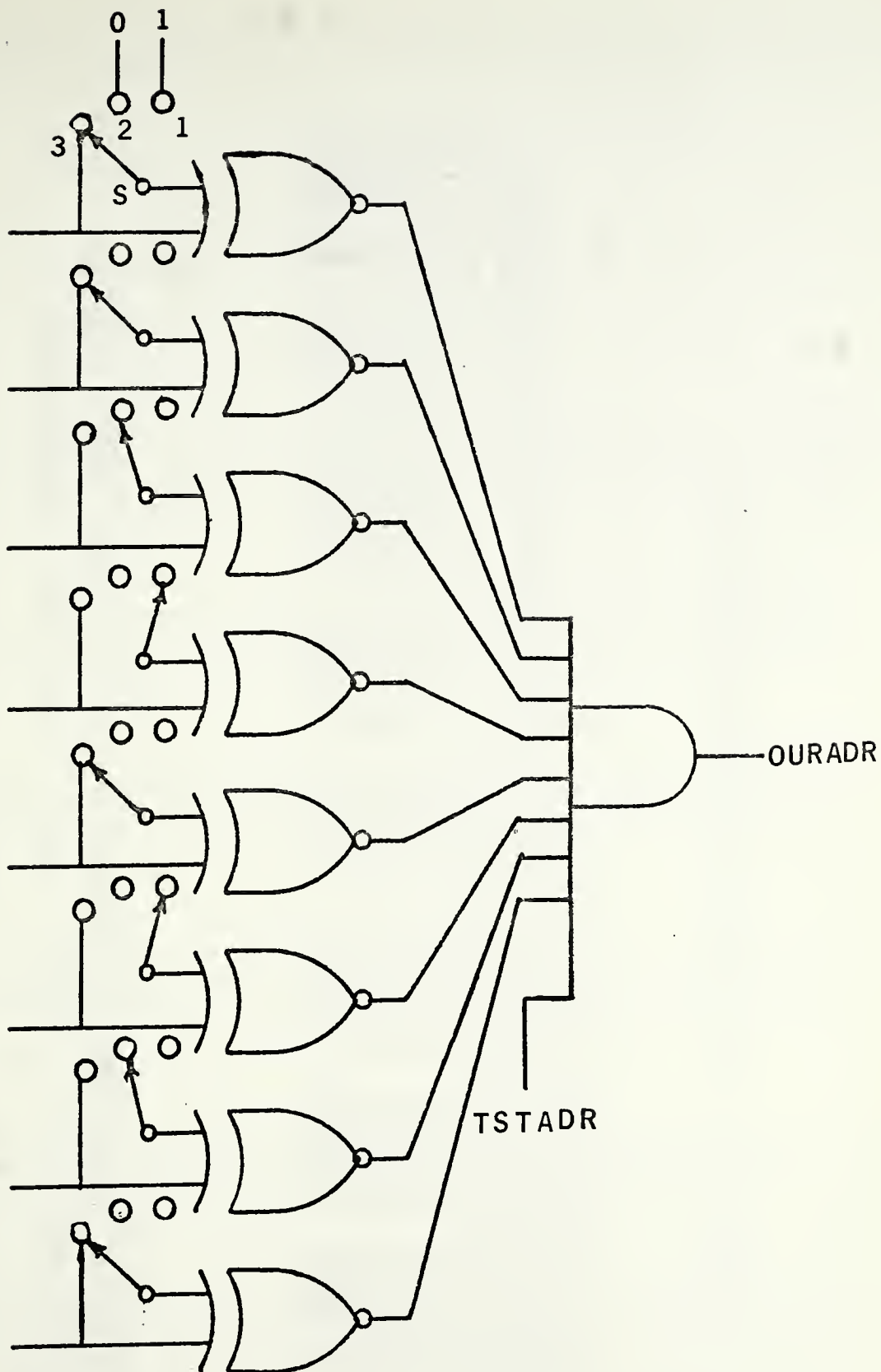


Figure 9. Address-checking function

1 3, 5, 4, 7, SELOUT, SUPOUT, COMOUT, SEROUT, CUBUSY, CHSEQ, CURADR,
 0, STAIN.
 0, CHSEQ, DCHSEQ, PSELOUT, DPSELOUT, DATABUSIN, DSERIN, SERIN, ADRBUSIN,
 DADRIN, ADRIN, STABUSIN, DSTAIN, STAIN, OPLIN, DCPLIN, DREQIN, TSTADR.

(A)

2 3, 5, 4, 7, 1, 000000, 2, 000001, 3, 000001, 4, 000010, 5, 000010, 6, 000011, 7, 000011,
 8, 001000, 9, 001000, 10, 001001, 11, 001001, 12, 001010, 13, 001010, 14, 001011, 15, 001011,
 16, 010000, 17, 010000, 18, 010001, 19, 010001, 20, 010010, 21, 010010, 22, 010011, 23, 010011,
 24, 011000, 25, 011000, 26, 011001, 27, 011001, 28, 011010, 29, 011010, 30, 011011, 31, 011011,
 32, 100000, 33, 100000, 34, 100001, 35, 100001, 36, 100010, 37, 100010, 38, 100011, 39, 100011,
 40, 101000, 41, 101000, 42, 101001, 43, 101001, 44, 101010, 45, 101010, 46, 101011, 47, 101011,
 48, 110000, 49, 110000, 50, 110001, 51, 110001, 52, 110010, 53, 110010, 54, 110011, 55, 110011,
 56, 111000, 57, 111000, 58, 111001, 59, 111001, 60, 111010, 61, 111010, 62, 111011, 63, 111011,
 0, 000001, 0001, ADROUT, 0010, SELOUT, 0011, SUPOUT, 0100, COMOUT, 0101, SEROUT, 0110, CUBUSY
 0, 0111, CHSEQ, 1000, CURADR, 1001, STAIN, 1010, PSELOUT, 0000010, DPSELOUT, 0000100, DATABUSI
 0, 000000, CHSEQ, 0000001, DCHSEQ, 0000010, DCHSEQ, 0000100, DADRIN, 0001001, ADRIN,
 N, 0000101, DSERIN, 0000110, DSTAIN, 0000110, STAIN, 0001101, DCPLIN, 0001110, DCPLIN,
 0, 001010, STABUSIN, 0001011, DSTAIN, 0001100, STAIN, 0001101, DCPLIN, 0001110, DCPLIN,
 0001111, DREQIN, 0010000, TSTADR, 0010001.

(B)

FIGURE 10. INPUT TO/OUTPUT FROM THE DATA GENERATOR

DATA	NF	/	3/	FWIDTH	/	5,	4,	7/
DATA	START	/	1,	504,	614,	04000/	514,	
DATA	MEMORY	/		258,				
1	514,			514,				514,
	514,			516,				514,
	1282,			514,				515,
	515,			514,				1794,
	520,			514,				515,
	514,			514,				522,
	514,			771,				515,
	2818,			515,				515,
	515,			515,				771,
	515,			771,				1282,
	770,			1538,				515,
	771,			515,				771,
	1794,			515,				771,
	770,			514,				2562,
	514,			771,				770,
	771,			2818,				772,
	514,			770,				1282,
	771,			772,				771,
	772,			1538,				514,
	1794,			771,				772,
	771,			515,				2562,
	515,			772,				771,
	772,			2818,				773,
	514,			771,				1283,
	514,			773,				515,
	773,			1539,				773,
	1795,			514,				2563,
	514,			770,				514,
	770,			773,				774,
	773,			2819,				514,
	515,			514,				774,
	515,			774,				1283,
	515,			774,				515,
	774,			1539,				770,
	1795,			515,				774,
	515,			771,				2563,
	771,			774,				770,
	774,			2819,				515,
	515,			770,				775,
	770,			775,				1283,
	775,			1539,				770,
	1795,			514,				771,
	771,							775,

770,	514,
514,	770,
514,	514,
514,	770,
2306,	770,
770,	771,
771,	770,
515,	770,
770,	771,
2050,	770,
770,	515,
515,	772,
772,	770,
770,	771,
771,	772,
2050,	771,
771,	770,
770,	773,
514,	514,
514,	773,
2051,	514,
514,	771,
771,	774,
774,	771,
515,	515,
774,	774,
2051,	515,
515,	514,
514,	775,
775,	771,
770,	770,
775,	775,
2051,	771,

770,	514,
514,	770,
514,	514,
514,	770,
770,	514,
514,	771,
1026,	771,
515,	1026,
771,	515,
2306,	771,
515,	2306,
772,	515,
770,	772,
771,	1026,
772,	770,
2306,	772,
514,	514,
772,	772,
2306,	771,
771,	770,
773,	773,
1027,	1027,
514,	514,
515,	515,
773,	773,
2307,	2307,
514,	514,
771,	771,
774,	774,
1027,	1027,
515,	515,
770,	770,
774,	774,
2307,	2307,
770,	770,
514,	514,
775,	775,
771,	771,
1027,	1027,
770,	770,
771,	771,
775,	775,
2307,	2307,

[illegible]

FIGURE 11. OUTPUT FROM THE TABLE GENERATOR

3

```

0 : 2, SEL OUT , DPSEL OUT .
1 : 38, 0 , TSTADR .
2 : 0, ADR CUT , .
3 : 4, SUP CUT , .
4 : 6, 0 , DREQ IN .
5 : 37, 1 , .
6 : 7, 1 , DCHSEQ .
7 : 8, 0 , OPLIN .
8 : 10, ADR OUT , ADR BUS IN .
10 : 12, COM OUT , ADR IN .
12 : 12, COM CUT , .
13 : 14, CHSEQ , DADR IN .
14 : 16, COM OUT , DATA BUS IN .
15 : 16, COM OUT , STABUS IN .
16 : 18, SER CUT , .
17 : 16, COM OUT , .
18 : 20, CHSEQ , .
19 : 18, SER CUT , .
20 : 22, COM OUT , SER IN .
22 : 24, SER CUT , .
23 : 32, STAIN , .
24 : 22, COM CUT , .
25 : 26, STAIN , .
26 : 28, SEL OUT , DSER IN .
27 : 30, 0 , .
28 : 0, ADR OUT , DOPLIN .
29 : 0, ADR OUT , .
30 : 28, SEL CUT , DSTAIN .
32 : 28, SEL CUT , DSER IN .
33 : 34, SEL CUT , DSTAIN .
34 : 0, ADR OUT , DOPLIN .
35 : 34, SEL CUT , .
36 : 22, COM CUT , .
37 : 0, ADR CUT , PSEL CUT .
40 : 0, ADR CUT , PSEL CUT .
41 : 42, SEL CUT , .
42 : 42, SEL CUT , .
43 : 44, CUBUSY , .
44 : 46, 0 , OPLIN .
45 : 47, 1 , STABUS IN .
46 : 10, ADR OUT , ADR BUS IN .
47 : 48, SEL CUT , STAIN .
48 : 50, ADR CUT , DSTAIN .
49 : 48, SEL OUT , .
50 : 0, ADR CUT , .
51 : 50, ADR CUT , .
*
```

FIGURE 12. THE MICROPROGRAM FOR THE INTERFACE

FOR EASE OF CHARACTER MANIPULATION, ALL PROGRAMS IN THIS SYSTEM USE A PARTICULAR CODE, IN WHICH ALL CHARACTERS ARE REPRESENTED BY INTEGER NUMBERS. THE TABLE BELOW IS THE MAPPING BETWEEN ACTUAL (INPUT/OUTPUT) CHARACTERS AND THE INTERNAL CODE.

ICC	CHAR	HEX	DEC	ICC	CHAR	HEX	DEC
1	BLANK	40	64	25	N	D5	213
2	0	F0	240	26	C	D6	214
3	1	F1	241	27	P	D7	215
4	2	F2	242	28	G	D8	216
5	3	F3	243	29	R	D9	217
6	4	F4	244	30	S	EE	227
7	5	F5	245	31	T	E3	228
8	6	F6	246	32	U	EE	229
9	7	F7	247	33	V	EE	230
10	8	F8	248	34	W	EE	231
11	9	F9	249	35	X	EE	232
12	A	C1	193	36	Y	EE	233
13	B	C2	194	37	Z	EE	234
14	C	C3	195	38	#	5B	51
15	D	C4	196	39	=	7E	126
16	E	C5	197	40	<	4B	75
17	F	C6	198	41	>	61	97
18	G	C7	199	42	(4D	77
19	H	C8	200	43)	5D	93
20	I	C9	201	44	-	4E	78
21	J	D1	209	45	:	6C	96
22	K	D2	210	46	*	7D	125
23	L	D3	211	47	,	5C	92
24	M	D4	212	48		6B	107

THE MAIN PROGRAM IS SIMPLY A DRIVER WHICH CALLS THE DATA GENERATOR, THE TABLE GENERATOR OF THE ASSEMBLER ACCORDING TO THE VALUE OF THE NUMBER READ ON THE FIRST CARD.

INITIALIZE VARIABLES.

```

CALL INIT
READ(5,100) I
FORMAT(11)
GC TO (1, 2, 3), I
1 GC TO DATGEN
2 GC TO 999
3 GC TO GENER
999 GC TO ASMAIN
STOP
END

```



```

BLCK DATA
INTEGER QTRAN, OBUFF, CBP, OUTREC, OUTLIM, FWIDTH
COMMON /INFO/ NF, FWIDTH(16), ISTART(16)
COMMON /MEMO/ MEMORY(2000), MEMBCT, MEMTOP, NDIV
COMMON /ICUNIT/ NREAD, NPRINT, NPUNCH
COMMON /TRANS/ ITRAN(256), OTRAN(64)
COMMON /BUFFER/ IBUFF(80), OBUFF(120), IBP, OBP
COMMON /MACHIN/ NBITS
COMMON /RECSZ/ OUTREC, OUTLIM
DATA OUTREC /80 /
DATA OBP/1/, IBP /81/
DATA NBITS /24/
DATA NREAD/5/, NPRINT/6/, NPUNCH/6/
DATA ITRAN/256 * 1H /
DATA OTRAN/1H, 1H0, 1H1, 1H2, 1H3, 1H4, 1H5, 1H6, 1H7, 1H8, 1H9, 1HA, 1HB, 1HC,
1HD, 1HE, 1HF, 1HG, 1HH, 1HI, 1HJ, 1HK, 1HL, 1HM, 1HN, 1HO, 1HP, 1HQ, 1HR, 1HS, 1
1HT, 1HU, 1HV, 1HW, 1HX, 1HY, 1HZ, 1H$, 1H=, 1H-, 1H<, 1H(, 1H), 1H>, 1H~, 1H*,
2, 1H, 1H /, 1H, 1H, 1H, 1H, 1H, 1H, 1H, 1H, 1H, 1H, 1H, 1H, 1H, 1H, 1H, 1H, 1H,
31H /
THE OUTPUT OF THE TABLE GENERATOR SHOULD BE INSERTED RIGHT AFTER
THIS COMMENT.
DATA MEMORY / 2000 * 0 /
END

```

CC

SUBROUTINE DATGEN

DATA GENERATOR MAIN

THIS SUBROUTINE HELPS PREPARING THE INPUT CARDS TO THE TABLE GENERATOR.

INTEGER FWIDTH, CONV, ACCUM, ACCLEN, TYPE
COMMON /ACUM/ ACCUM(32), ACCLEN, TYPE
COMMON /ICUNIT/ NREAD, NPRINT, NPUNCH
DIMENSION FWIDTH(16)

FPCM NOW ON OUTPUT IS ON THE CARDPUNCH.

NPRINT = 7
NPUNCH = 7
CALL PAD(1, 4, 1)
CALL WRITEL(0, NPUNCH)

GET THE NUMBER OF FIELDS IN EACH WORD .

CALL SCAN
NF = CONV(M)

GET THE NUMBER OF BITS IN EACH FIELD.

DO 400 I = 1, NF
CALL SCAN
FWIDTH(I) = CONV(M)
CONTINUE

400

OUTPUT THE NUMBER OF FIELDS IN EACH WORD.

CALL CONGUT(1, -2, NF, 10)
CALL PAD(1, 48, 1)

OUTPUT THE NUMBER OF BITS IN EACH FIELD.

DO 402 I = 1, NF
CALL CONGUT(1, -2, FWIDTH(I), 10)
CALL PAD(1, 48, 1)
CONTINUE

402

CALL WRITEL(0, NPUNCH)

GENERATE AND OUTPUT THE CODE CORRESPONDING TO THE
'NEXT BASIC ADDRESS' FIELD.

C

```

NFW = FWIDTH(1)
LIM = 2 ** (NFW + 1)
I = 0
GO TO 3
CALL PAD(1, 48, 1)
J = I / 2
CALL CONOUT(1, -3, I, 10)
CALL PAD(1, 48, 1)
CALL CONOUT(1, NFW, J, 2)
I = I + 1
IF (I .LT. LIM) GO TO 4
CALL PAD(1, 40, 1)
CALL WRITE(0, NPRINT)

```

C

READ EACH MNEMONIC, GENERATE ITS CODE AND OUTPUT BOTH.

```

DO 401 K = 2, NF
I = 0
GO TO 1
CALL PAD(1, 48, 1)
CALL SCAN
J = ACLEN - 1
CALL FORM(1, ACCUM, 1, J, 32)
CALL PAD(1, 48, 1)
CALL CONOUT(1, FWIDTH(K), I, 2)
I = I + 1
IF (I TYPE .NE. 3) GO TO 5
CALL PAD(1, 40, 1)
CALL WRITE(0, NPUNCH)
CONTINUE

```

```

401 STOP
END

```



```

SUBROUTINE GENER
C
C
C      TABLE GENERATOR MAIN
C
INTEGER OUTMSG, FWIDTH, TYPE, ACCLEN, ACCUM, OBUFF, CBP
INTEGER GET, CONV
INTEGER OUTREC, OUTLIM
DIMENSION OUTMSG(34)
COMMON /BUFFER/ IBUFF(80), OBUFF(120), IBP, CBP
COMMON /UNIT/ NREAD, NPRINT, NPUNCH
COMMON /MEMO/ MEMRY(2000), MEMBCT, MEMTCP, NDIV
COMMON /ACUM/ ACCUM(32), ACCLEN, TYPE
COMMON /RECSZ/ OUTREC, OUTLIM
COMMON /INFO/ NF, FWIDTH(16), ISTART(16)
DATA OUTMSG/15, 12, 31, 12, 1, 24, 16, 24,
1 49, 20, 30, 31, 12, 29, 31, 49, 25, 17, 1, 49, 17, 34, 20,
215, 31, 19, 1, 49 /
C
C      READ NUMBER OF FIELDS AND NUMBER OF BITS CONTAINED IN EACH FIELD.
C
CALL SCAN
NF = CONV(M)
DO 0400 I = 1, NF
CALL SCAN
FWIDTH(I) = CONV(M)
CONTINUE
NPRINT = 7
NPUNCH = 7
CALL PAD(1, 1, 6)
CALL FORM(1, OUTMSG, 1, 5, 34)
CALL FORM(1, OUTMSG, 21, 24, 34)
CALL CONOUT(1, -3, NF, 10)
CALL PAD(1, 49, 1)
CALL PAD(1, 48, 1)
CALL FORM(1, OUTMSG, 25, 32, 34)
DO 406 I = 1, NF
CALL CONOUT(1, -3, FWIDTH(I), 10)
IF (I.EQ. NF) GO TO 2
CALL PAD(1, 48, 1)
CONTINUE
406 CALL PAD(1, 49, 1)
2 CALL WRITEL(0, NPUNCH)
C
C      READ ALL LEGAL INPUTS AND CORRESPONDING CCDE TO BE PRODUCED,
C      FIELD BY FIELD.
C
DO 0401 I = 1, NF

```



```

C C   SAVE THE LOCATION WHERE THE TABLE FOR THIS FIELD STARTS.
C C   ISTART(I) = MEMBOT
C C
C C   MAKE THE EMPTY INPUT CORRESPOND TO CODE C.
C C
C C   CALL PUT(MEMBOT,1)
C C   K = FWIDTH(I)
C C   DO 0405 J = 1, K
C C   CALL PUT(MEMBOT, 2)
C C   CONTINUE
0405
C C   GET THE NEXT ELEMENT.
C C
C C   CALL SCAN
0001
C C   IF THE INPUT CONTAINS A '.' IN THE FIRST PLACE, THAT IS ALL
C C   THERE IS FOR THE CURRENT FIELD.
C C
C C   IF (TYPE .EQ. 3) GO TO 0401
C C   STORE THE LENGTH OF THIS ELEMENT.
C C
C C   CALL PUT(MEMBOT, ACCLEN)
C C   STORE THE ELEMENT IN 'MEMORY',
C C
C C   K = ACCLEN - 1
C C   DO 0402 J = 1, K
C C   CALL PUT(MEMBOT, ACCUM(J))
C C   CONTINUE
0402
C C   GET THE CORRESPONDING CODE.
C C
C C   CALL SCAN
C C   IF (TYPE .EQ. 3) GO TO 0401
C C   STORE IT INTO 'MEMORY'.
C C
C C   K = ACCLEN - 1
C C   DO 0403 J = 1, K
C C   CALL PUT(MEMBOT, ACCUM(J))
C C   CONTINUE
C C   GO TO 1
0403
0401
C C   NOW DUMP 'ISTART'.
C C

```



```

OUTREC = 72
OUTLIM = 73
CALL PAD(1, 1, 6)
CALL FORM(1, OUTMSG, 1, 5, 34)
CALL FORM(1, OUTMSG, 14, 20, 34)
I = 1
0006 CALL CONOUT(1, -4, ISTART(1), 10)
I = I + 1
IF(I.GT. NF) GO TO 7
CALL PAD(1, 48, 1)
IF(OBP.LT. 68) GO TO 6
CALL WRITEL(0, NPUNCH)
CALL PAD(1, 1, 5)
CALL PAD(1, 3, 1)
GO TO 6
0007 CALL PAD(1, 48, 1)
CALL CONOUT(1, 5, 4000, 10)
CALL PAD(1, 49, 1)
CALL WRITEL(0, NPUNCH)
DUMP 'MEMORY'.
CALL PAD(1, 1, 6)
CALL FORM(1, OUTMSG, 1, 5, 34)
CALL FORM(1, OUTMSG, 6, 13, 34)
LIM = MEMBOT / NDIV + 1
I = 1
0004 CALL CONOUT(1, -10, MEMORY(1), 10)
I = I + 1
IF(I.GT. LIM) GO TO 5
CALL PAD(1, 48, 1)
IF(OBP.LT. 62) GO TO 4
CALL WRITEL(0, NPUNCH)
CALL PAD(1, 1, 5)
CALL PAD(1, 3, 1)
GO TO 4
0005 CALL PAD(1, 49, 1)
CALL WRITEL(0, NPUNCH)
RETURN
END

```



```

C
C
SUBROUTINE ASMAIN
      ASSEMBLER MAIN
      INTEGER DIGIT
      INTEGER TYPE, VALUE, CONV, FIELD, TEMP1, TEMP2, FWIDTH, GET,
1  ACCLEN, ACCUM, CODE, ZERO
      DIMENSION ISTART(16), FWIDTH(16), CODE(16), ZERO(1)
      COMMON /MEMO/ MEMORY(2000), MEMBCT, MEMTOP, NDIV
      COMMON /ACUM/ ACCUM(32), ACCLEN, TYPE
      COMMON /ICUNIT/ NREAD, NPRINT, NPUNCH
      DATA ZERO /1/
      DATA ISTART/ 1, 504, 618, 843 /
      DATA FWIDTH / 5, 4, 7 /
      INITIALIZE
      MEMTOP = 4000
      KP = 7
      KODE = 0
      L = 0
      LABEL = -1
      WRITE(6, 363)
      FORMAT(IH1)
363
      GET THE NEXT ELEMENT.
      CALL SCAN
0004
      SEE 'SCAN' FOR DEFINITION OF 'TYPE' VALUES.
      GO TO (1, 2, 2, 12), TYPE
      THE ELEMENT IS A <LABEL>. CHECK FOR SEQUENCE GAP.
0001 VALUE = CONV(M)
0013 LABEL = LABEL + 1
      IF (VALUE .EQ. LABEL) GO TO 0005
      THERE IS A SEQUENCE GAP.
      CALL PUT(-MEMTOP, 0)
      CALL PUT(-MEMTOP, 0)
      GO TO 0013
      NOW GET THE CONTENTS OF FIELD 1.
C
C
C
C

```



```

0005 FIELD = 1
GO TO 0004
C
C THE ELEMENT IS AN IDENTIFIER .FIND IT IN THE LIST.
C
0002 I = ISTART(FIELD)
TEMP1 = FWIDTH(FIELD)
0007 IF (ACCLN.EQ. 1) GO TO 0006
TEMP2 = GET(I)
0011 I = I + TEMP2 + TEMP1
IF (I.LT. ISTART(FIELD+1)) GO TO 007
CALL ERRCR(39)
GO TO 0012
C
C THE LENGTHS AGREE. CHECK ALL CHARACTERS, ONE AT A TIME.
C
0006 J = 1
K = I + 1
IF (ACCLN.EQ. 1) GO TO 10
IF (ACCU(J).NE. GET(K)) GO TO 0011
0009 J = J + 1
K = K + 1
IF (J.LT. ACCLN) GO TO 0009
C
C WE FOUND IT. GET THE CORRESPONDING CODE.
C
0010 LIM = 1
L = 1
K + TEMP1 - 1
DO 403 KI = K,LIM
CODE = CODE + (GET(KI) - 2) * 2 ** KP
KP = KP - 1
IF (KP.GE. 0) GO TO 403
CALL PUT(-MEMTOP, CODE)
IF (MEMTOP.LE. MEMBOT) CALL ERROR (27)
KP = 7
CODE = 0
CCONTINUE
0403 IF (TYPE.LE. 2) FIELD = FIELD + 1
GO TO 4
12 CALL PUNCH
0999 RETURN
END

```



```

SUBROUTINE INIT
THIS SUBPROGRAM INITIALIZES ALL THE TABLES AND VARIABLES FOR
USE OF THE SYSTEM.

MEANING OF VARIABLES:
VIRTUAL MEMORY USED BY THE SYSTEM. EACH COMPUTER WORD
IN MEMORY IS SUBDIVIDED IN 'NDIV' SUBDIVISIONS.
OUTREC SIZE OF THE OUTPUT RECORD
OUTLIM EQUAL TO OUTREC + 1 IS USED AS TESTING PARAMETER.
OTRAN VECTOR OF LENGTH 64 CONTAINS ALL THE CHARACTERS THAT
WILL BE RECOGNIZED BY THE SYSTEM.
NDIV NUMBER OF DIVISIONS WITHIN A COMPUTER WORD FOR USE
AS VIRTUAL STORAGE.
NBITS NUMBER OF BITS IN ONE WORD (THIS VALUE IS TO BE MODIFIED
FOR USE ON DIFFERENT COMPUTERS IF MAXIMUM EFFICIENCY
OF MEMORY USE IS TO BE OBTAINED.
MEMBOT POINTER TO THE HIGHER LOCATION IN VIRTUAL MEMORY NOT YET
USED.
ITRAN VECTOR OF LENGTH 256 CONTAINS ALL THE CODES FOR THE
CHARACTERS RECOGNIZED BY THE SYSTEM.
ICGN SUBPROGRAM THAT, GIVEN A CHARACTER, RETURNS ITS CODE.

INTEGER OUTREC, OUTLIM, OTRAN
COMMON /MEMO/ MEMORY(2000), MEMBOT, MEMTOP, NDIV
COMMON /TRANS/ ITRAN(256), OTRAN(64)
COMMON /MACHIN/ NBITS
COMMON /RECSZ/ OUTREC, OUTLIM

OUTLIM = OUTREC + 1
NDIV = (NBITS - 1) / 8
MEMBOT = 1

SET UP ITRAN (INPUT TRANSLATOR TABLE).

DO 0400 I = 1, 49
  J = OTRAN (I)
  J = ICGN (J)
  ITRAN(J) = I
CONTINUE
RETURN
END
0400

```



```

C C C C
INTEGER FUNCTION CCNV(PREC)
THIS SUBPROGRAM TAKES A NUMBER IN THE ACCUMULATOR ('ACCUM') AND
CCNVERTS IT TO THE NORMAL BINARY MACHINE REPRESENTATION.

C C C C
INTEGER PREC, DIGIT
INTEGER ACCUM, ACCLEN, TYPE
COMMON /ACUM/ ACCUM(32), ACCLEN, TYPE

C C C C
INITIALIZE
CCNV = 0
PREC = 0
I = ACCLEN - 1

C C C C
GET THE LEAST SIGNIFICANT DIGIT AND DECODE IT.

1 DIGIT = ACCUM(I) - 2
IF (DIGIT .GT. 9) CALL ERROR(14)

C C C C
UPDATE 'CONV'
CCNV = CCNV + DIGIT * 10 ** (ACCLEN - 1 - I)
PREC = PREC + 1
I = I - 1

C C C C
IF THERE ARE MORE DIGITS, DO IT AGAIN
IF (I .NE. 0) GO TO 1
RETURN
END

```



```

C C C C C C C C
SUBROUTINE CONOUT(CC, FIELDW, VAL, BASE)
THIS SUBPROGRAM PLACES THE VALUE OF 'VAL' INTO THE OUTPUT BUFFER
IN A FIELD WIDTH OF 'FIELDW' USING THE RADIX 'BASE'. IF 'FIELDW'
IS NEGATIVE, SUPPRESS LEADING ZERCS.

INTEGER OBUFF, OBP, OUTREC, OUTLIM
INTEGER TEMP, CC, FIELDW, VAL, BASE, PTR
COMMON /ICUNIT/ NREAD, NPRINT, NPUNCH
COMMON /BUFFER/ IBUFF(80), OBUFF(120), IBP, OBP
COMMON /RECSZ/ OUTREC, OUTLIM

TEMP = IABS(VAL)

IF 'CC' = 0 DUMP CURRENT 'OBUFF' AND START A NEW LINE.
IF (CC .EQ. 0) CALL WRITEL(0, NPRINT)
SET A POINTER TO THE END OF THE FIELD.
PTR = OBP + IABS(FIELDW) - 1
IF THE NUMBER WILL NOT FIT IN THIS RECORD, START A NEW CNE.
IF (PTR .LT. OUTLIM) GO TO 4
CALL WRITEL(0, NPRINT)
PTR = IABS(FIELDW)
CCPY THE LOWER LIMIT OF THE FIELDW INTO 'LCWR'.
4 LCWR = OBP

SET 'OBP' TO THE FIRST SPACE AVAILABLE AFTER THE NUMBER
OBP = PTR + 1
GET THE RIGHTMOST DIGIT FROM 'VAL'.
1 NDIG = MOD (TEMP, BASE)
CCDE IT INTO INTERMEDIATE CODE.
NDIG = NDIG + 2
CHECK TO SEE IF THERE IS STILL ROOM IN THE FIELD.
IF (PTR .LT. LOWER) GO TO 2

```



```

C C STORE IT INTO 'OBUFF'.
C C OBUFF(PTR) = NDIG
C C PTR = PTR - 1
C C DROP THE RIGHTMOST DIGIT OF 'VAL'.
C C TEMP = TEMP / BASE
C C WAS THIS THE MOST SIGNIFICANT DIGIT OF 'VAL' ?
C C IF (TEMP .NE. 0) GO TO 1
C C IF (PTR .LT. LOWER) GO TO 3
C C FILL THE LEADING SPACES WITH ZEROS (IF 'FIELDW' < 0)
C C OR BLANKS.
C C KAR = 2
C C IF (FIELDW .LT. 0) KAR = 1
C C L = PTR
C C DO 400 PTR = LOWER, L
C C OBUFF(PTR) = KAR
C C CONTINUE
C C 400 GC TO 3
C C 2 CALL ERROR(20)
C C 3 RETURN
C C END

```



```

SUBROUTINE PAD(CC, CHR, NCHRS)
THIS SUBPROGRAM PLACES THE CHARACTER 'CHR' REPEATED 'NCHRS' TIMES
INTO THE OUTPUT BUFFER.
MEANING OF VARIABLES:
CC      CARRIAGE CONTROL. IF = 0 DUMP CURRENT BUFFER FIRST.
CHR     CHARACTER TO BE INSERTED INTO 'CBUFF'.
CBUFF   CHARACTER BUFFER.
CBP     CURRENT BUFFER POSITION.
NCHRS   NUMBER OF TIMES 'CHR' IS TO BE REPEATED.
INTEGER OBUFF, OBP, OUTREC, OUTLIM
INTEGER CC, CHR
COMMON /ICOUNT/ NREAD, NPRINT, NPUNCH
COMMON /IBUFFER/ IBUFF(80), OBUFF(120), IBP, OBP
COMMON /RECSZ/ OUTREC, OUTLIM

IF (CC .EQ. 0) CALL WRITEL(0,NPRINT)

DO 7400 I = 1, NCHRS
  IF (OBP .EQ. OUTLIM) CALL WRITEL(0,NPRINT )
  OBUFF(OBP) = CHR
  OBP = OBP + 1
CONTINUE
7400 RETURN
END

```


SUBROUTINE FORM(CC, CHARS, START, FINISH, LEN)
 THIS SUBPROGRAM PLACES THE CHARACTERS FROM 'CHARS', INTO THE OUTPUT
 BUFFER STARTING AT 'CHARS(START)', AND ENDING AT 'CHARS(FINISH)'.
 CCCCCCCCCCCCCCCCCC

MEANING OF VARIABLES:

CC CARRIAGE CONTROL. IF 'CC' = 0 DUMP CURRENT 'OBUFF' AND
 START A NEW LINE.
 CHARS VECTOR OF LENGTH 'LEN' IF CC=1 APPEND TO CURRENT 'OBUFF'.
 BE PLACED IN 'OBUFF'. WHICH CONTAINS THE CHARACTERS TO
 START BE PLACED IN 'OBUFF'.
 FINISH PCOUNTER TO THE FIRST MEMBER OF 'CHARS' TO GET OUT.
 LEN POINTER TO THE LAST MEMBER OF 'CHARS' TO GET OUT.
 LENGTH. DIMENSION OF 'CHARS'.

INTEGER OBUFF, OBP, OUTREC, OUTLIM
 INTEGER CC, CHARS, START, FINISH
 COMMON /ICUNIT/ NREAD, NPRINT, NPUNCH
 COMMON /BUFFER/ IBUFF(80), OBUFF(120), IBP, OBP
 COMMON /RECSZ/ OUTREC, OUTLIM
 DIMENSION CHARS(LEN)

IF 'CC' = 0 START A NEW LINE.
 IF (CC .EQ. 0) CALL WRITEL(0, NPRINT)
 PLACE DESIRED INFORMATION INTO 'OBUFF'.

1 I = START
 OBUFF(OBP) = CHARS(I)
 OBP = OBP + 1
 IF (OBP .EQ. OUTLIM) CALL WRITEL(0, NPRINT)
 I = I + 1
 IF (I .LE. FINISH) GO TO 1
 RETURN
 END

CCCC


```

SUBROUTINE WRITEL(NLINE, NUNIT)
THIS SUBPROGRAM OUTPUTS THE CURRENT OUTPUT BUFFER VIA I/C UNIT
•NUNIT• AND APPENDS •NLINE• BLANK RECORDS.
MEANING OF VARIABLES:
NLINE      NUMBER OF LINES (OR RECCRDS) TO BE INSERTED AFTER
            OUTPUTTING THE CURRENT OUTPUT BUFFER.
NLNIT      LOGICAL NUMBER OF OUTPUT UNIT TO BE USED.
INTEGER QTRAN, OBUFF, OBP, OUTREC, CUTLIM
INTEGER TEMP
COMMON /ICUNIT/ NREAD, NPRINT, NPUNCH
COMMON /TRANS/ ITRAN(256), OTRAN(64)
COMMON /BUFFER/ IBUFF(80), OBUFF(120), IBP, OBP
COMMON /RECSZ/ OUTREC, OUTLIM
IF 'OBUFF' IS NOT COMPLETELY FULL, PAD WITH BLANKS.
IF (OBP .EQ. CUTLIM) GO TO 6001
TEMP = CUTLIM - OBP
CALL PAD (1, 1, TEMP)
DECODE 'OBUFF'.
        DC 6400 I = 1, OUTREC
        OBUFF(I) = OTRAN(OBUFF(I))
        CONTINUE
        NCW DUMP IT.
IF (NUNIT .NE. 7) GO TO 6004
WRITE(NUNIT, 6103) (OBUFF(I), I = 1, OUTREC)
FCRMAT (120A1)
GC TO 6003
6004 WRITE(NUNIT, 6100) (OBUFF(I), I=1, OUTREC)
6100 FCRMAT(1X, 120A1)
        RESET OBP.
        6003 OBP = 1
SEE IF THERE ARE BLANK RECORDS TO BE INSERTED.
IF (NLINE .EQ. 0) GO TO 6002
DO 6401 I = 1, NLINE
    WRITE (NUNIT, 6101)

```


6101 FORMAT(1H)
6401 CONTINUE
6002 RETURN
 END

SUBROUTINE SCAN

THIS SUBROUTINE :
 A) GETS THE NEXT ELEMENT IN THE INPUT STREAM (CHARACTER BY CHARACTER, IGNORING BLANKS).
 B) STORES IT, ALREADY CODED INTO INTERMEDIATE CODE (AN INTEGER BETWEEN 1 AND 64 FOR EACH CHARACTER) INTO AN ACCUMULATOR.
 C) GETS THE NEXT SYMBOL, WHICH SHOULD BE ONE OF THE SPECIAL CHARACTERS USED AS <DELIMITER>
 D) RETURNS THE ACCUMULATOR AND THE TYPE OF ELEMENT IN IT TO THE CALLING PROGRAM.
 E) ISSUES ERROR MESSAGES WHENEVER APPROPRIATE.

MEANING OF VARIABLES:

NC NEXT CHARACTER IN THE INPUT STREAM
 ACCUM ACCUMULATOR. VECTOR OF LENGTH 32 USED TO HOLD THE ELEMENT BEING ANALYZED.
 ACCLEN ACCUMULATOR LENGTH. POINTER TO 'ACCUM' TELLS HOW LONG IS THE ELEMENT SCFAR.
 TYPE IF TYPE = 1 THEN THE ELEMENT IS A LABEL.
 IF TYPE = 2 THEN THE ELEMENT IS AN IDENTIFIER.
 IF TYPE = 3 THEN THE ELEMENT IS THE LAST IDENTIFIER IN THIS STATEMENT.
 IF TYPE = 4 THIS IS THE LAST CARD IN THE PROGRAM.

INTEGER ACCUM, ACCLEN, TYPE
 INTEGER GNC
 COMMON /ACUM/ ACCUM(32), ACCLEN, TYPE

RESET 'ACCLEN'.

ACCLEN = 1

GET A CHARACTER FROM INPUT STREAM.

NC = GNC(0)

IS IT AN ALPHANUMERIC CHARACTER ('\$', INCLUSIVE) ? IF NOT, GO TO 3003.

IF (NC .GT. 38) GO TO 3003

IF 'NC' = 0 IT IS TIME TO STOP.

IF (NC .NE. 0) GO TO 3001
 TYPE = 4
 GC TO 3009


```

C
C
C 3001
C
C WE FOUND AN IDENTIFIER. COPY IT INTO 'ACCUM'.
C
C ACCUM(ACCLEN) = NC
C ACCLEN = ACCLEN + 1
C IF (ACCLEN .LT. 33) GO TO 3002
C CALL ERROR(18)
C GO TO 3009
C
C WE FOUND A SPECIAL CHARACTER. THERE ARE FOUR LEGAL CASES:
C A) A COMMA(48) MEANING THAT WE HAVE AN IDENTIFIER IN 'ACCUM'.
C B) A COLON(46) MEANING THAT WE HAVE A LABEL IN 'ACCUM'.
C C) A PERIOD(40) MEANING THAT THE IDENTIFIER IN 'ACCUM' IS THE
C LAST IN THIS STATEMENT.
C D) A 'LESS THAN' SIGN(41) MEANING THAT WHAT FOLLOWS IS A COMMENT.
C
C 3003 IF (NC .NE. 48) GO TO 3004
C
C WE FOUND A COMMA ; SET 'TYPE' = 2 AND RETURN.
C
C TYPE = 2
C GO TO 3009
C 3004 IF (NC .NE. 46) GO TO 3005
C
C WE FOUND A COLON ; SET 'TYPE' = 1 AND RETURN.
C
C TYPE = 1
C GO TO 3009
C 3005 IF (NC .NE. 40) GO TO 3006
C
C TYPE = 3
C GO TO 3009
C 3006 IF (NC .NE. 41) GO TO 3007
C
C 3011 NC = GNC(0)
C IF (NC .NE. 44) GO TO 3011
C GO TO 3002
C CALL ERROR (19)
C RETURN
C END

```


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1003

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1100 1101

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1001

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```

C C C NC = ICGN(NC)
C C C NC = ITRAN(NC)
C C C GET RID OF IT IF IT IS A BLANK.
C C C IF (NC .EQ. 1) GO TO 1003
C C C THE FIRST CHARACTER ON A CARD GETS SPECIAL ATTENTION, AS IT COULD
C C C BE AN END OF FILE MARK.
C C C IF (IBP .NE. 2 ) GO TO 1002
C C C IF THE FIRST CHARACTER IN THE CARD IS A '*' 'GNC' MUST BE SET
C C C TO ZERO.
C C C IF (NC .EQ. 47) NC = 0
C C C GNC = NC
C C C RETURN
C C C END
C C C 1002

```


CCCCCCCCCCCC CCCC CCCC CCCC CCCC
 INTEGER FUNCTION GET(LOC)
 THIS SUBPROGRAM GETS THE POSITIVE INTEGER NUMBER , LESS THAN
 256 , STORED IN VIRTUAL MEMORY ADDRESS 'LCC'.

MEANING OF VARIABLES:

ADD REAL MEMORY ADDRESS WHICH CONTAINS 'LOC'.
 TEMP AUXILIARY VARIABLE USE TO HOLD TEMPORARY VALUES.
 TEMP1 AUXILIARY VARIABLE USE TO HOLD TEMPORARY VALUES.

INTEGER ADD, TEMP, TEMP1
 COMMON /MEMO/ MEMORY(2000), MEMBCT, MEMTOP, NDIV
 GET THE REAL MEMORY ADDRESS CORRESPONDING TO 'LOC'.

ADD = (LOC - 1) / NDIV + 1

COPY ITS CONTENTS TO MAKE EXECUTION FASTER.

TEMP = MEMORY(ADD)

LOCATE 'LOC' INSIDE THE ADDRESS 'ADD'.

TEMP1 = LOC - ((ADD - 1) * NDIV)
 TEMP1 = NDIV - TEMP1
 TEMP1 = 256 * TEMP1
 TEMP = TEMP / TEMP1
 GET = MGD(TEMP, 256)
 RETURN
 END


```

SUBROUTINE PUT(LOC, VAL)

THIS SUBPROGRAM STORES AN INTEGER NUMBER 'VAL' (BETWEEN 0 AND 255)
INTO 8 BITS OF A COMPUTER WORD
THIS IS DONE TO SAVE STORAGE SPACE.

MEANING OF VARIABLES:

LOC      LOCATION IN THE 'VIRTUAL MEMORY' WHERE THE VALUE IS TO
          BE STORED. IF POSITIVE, INCREMENT 'MEMBOT'. IF NEGATIVE
          DECREMENT 'MEMTOP'.
VAL      INTEGER VALUE TO BE STORED IN 'LOC'.
MEMBOT   MEMORY BOTTOM. POINTER TO THE LOWEST NUMBERED VIRTUAL
          ADDRESS AVAILABLE.
MEMTOP   MEMORY TOP. POINTER TO THE HIGHEST NUMBERED VIRTUAL
          ADDRESS AVAILABLE.
INCR      INCREMENT. ADDS 1 TO 'MEMBOT' OR SUBTRACTS 1 FROM
          'MEMTOP' DEPENDING UPON THE SIGN OF 'LOC'.
ADD      REAL MEMORY ADDRESS WHICH CONTAINS 'LOC'.
TEMP     AUXILIARY VARIABLE TO HOLD TEMPORARY VALUES.
TEMP1    AUXILIARY VARIABLE TO HOLD TEMPORARY VALUES.
TEMP2    AUXILIARY VARIABLE TO HOLD TEMPORARY VALUES.
NDIV     NUMBER OF DIVISIONS (VIRTUAL MEMORY ADDRESSES)
          INSIDE A REAL MEMORY WORD.
SAV      CONTENTS OF REAL MEMORY WORD TO THE RIGHT OF 'LOC'.

INTEGER VAL, ADD, TEMP, TEMP1, TEMP2, SAV
COMMON /MEMO/ MEMORY(2000), MEMBOT, MEMTOP, NDIV

SET 'INCR' TO THE PROPER VALUE.

INCR = 1
IF (LOC .GT. 0) GO TO 5001
LOC = -LOC
INCR = -INCR

COMPUTE THE ACTUAL MEMORY WORD ADDRESS.

5001 ADD = (LOC - 1) / NDIV + 1
I F(ADD .GT. NDIV * 2000) CALL ERRCR(37)

CCPY THE CURRENT CONTENTS OF 'MEMORY(ADD)' TO SPEED UP COMPUTATION

TEMP = MEMORY (ADD)

FIND THE POSITION OF 'LOC' INSIDE THE WORD. IT WILL BE AN INTEGER
BETWEEN 1 AND NDIV.

```



```

TEMP1 = NDIV - (LOC - NDIV * (ADD - 1))
SAVE THE VALUES TO THE RIGHT OF 'LCC'.
TEMP1 = 256 ** TEMP1
SAV = MOD (TEMP, TEMP1)
TEMP2 = TEMP1 * 256
TEMP = (TEMP / TEMP2 * TEMP2 + VAL) * TEMP1 + SAV
MEMORY (ADD) = TEMP
LCC = LCC + INCR
RETURN
END

```

CC


```

C
C
C
C
C
C
SUBROUTINE PUNCH
THIS SUBROUTINE, CALLED AT THE END OF THE ASSEMBLER, DUMPS
THE CONTENTS OF MEMORY INTO A PAPER TAPE IN A FORMAT SUITABLE
TO PROGRAM A ROM. IT SHOULD BE REVISED WHENEVER CHANGES ARE MADE
TO THE TAPE PUNCH OR TO THE ROM PROGRAMMING SYSTEM.

INTEGER RUBOUT, B, P, F, GET
DATA RUBOUT/177/, B/102/, P/120/, N/116/, F/106/
KA = 4000
DO 400 I = 1,25
WRITE(7,100) RUBOUT
100 FORMAT(11)
DO 404 I = 1,256
WRITE(7,100) B
KCODE = GET(KA)
DO 405 J = 1,8
DIGIT = MOD(KCODE, 2)
KCODE = KCODE / 2
IF (DIGIT) 1,2,3
1 CALL ERROR(27)
RETURN
2 WRITE (7,100) N
GO TO 405
3 WRITE(7,100) P
CONTINUE
405 WRITE(7,100) F
KA = KA -- 2
CONTINUE
DO 408 I = 1,25
WRITE(7,100) RUBOUT
408 IF (MOD(KA,2) .NE. 0) GO TO 999
KA = 3599
GO TO 015
999 RETURN
END

```


SUBROUTINE ERROR(N)
 THIS SUBPROGRAM PRINTS AN ERROR MESSAGE IN THE FOLLOWING FORMAT:
 ERROR

ERROR MESSAGES

ERROR NUMBER	SUBPROGRAM CALLING	LINE IN SUBPROGRAM	INTERPRETATION
35	ASMAIN	64	IDENTIFIER NOT FOUND IN 'MEMORY'.
18	SCAN	62	IDENTIFIER TOO LONG (> 32 CHARACTERS).
19	SCAN	91	UNKNOWN SPECIAL CHARACTER.
20	CONOUT	75	NUMBER LARGER THAN FIELD PROVIDED.
37	PUT	48	MEMORY EXHAUSTED.

INTEGER ACCUM, ACCLEN, TYPE, OBUFF, OBP, CUTREC, OUTLIM
 INTEGER TEMP, SAVBUF, ERMMSG
 COMMON /ICUNIT/ NREAD, NPRINT, NPUNCH
 COMMON /ACUM/ ACCUM(32), ACCLEN, TYPE
 COMMON /BUFFER/ IBUFF(80), OBUFF(120), IBP, OBP
 COMMON /RECSZ/ CUTREC, OUTLIM
 DIMENSION SAVBUF(120), ERMMSG(26)
 DATA ERMMSG /16, 29, 29, 26, 29, 1, 25, 32, 24, 13, 16, 25, 1,
 1 20, 25, 1, 23, 20, 25, 16, 1, 25, 16, 12, 29, 1 /

SAVE CURRENT CONTENTS CF 'CBUFF'

```

DO 8400 I = 1, OUTREC
  SAVBUF(I) = OBUFF(I)
CONTINUE
TEMP = OBP
I = NPRINT
NPRINT = 6
OBP = 1
CALL PAD(1, 47, ERMMSG, 1, 5, 26)
CALL FCRM(1, 47, 3)
CALL PAD(1, 47, 3)
CALL PAD(1, 1, 5)
CALL FCRM(1, ERMMSG, 1, 13, 26)
CALL CONOUT(1, 4, N, 10)
CALL FCRM(1, ERMMSG, 13, 21, 26)
CALL CONOUT(1, 6, LINE, 10)
CALL FCRM(1, ERMMSG, 21, 26, 26)
M = ACCLEN - 1
CALL FCRM(1, ACCUM, 1, M, 32)
CALL WRITE(0, NPRINT)
DO 8401 I = 1, 120
  OBUFF(I) = SAVBUF(I)
CONTINUE

```

8401


```
NPRINT = I  
QBPP = TEMP  
RETURN  
END
```


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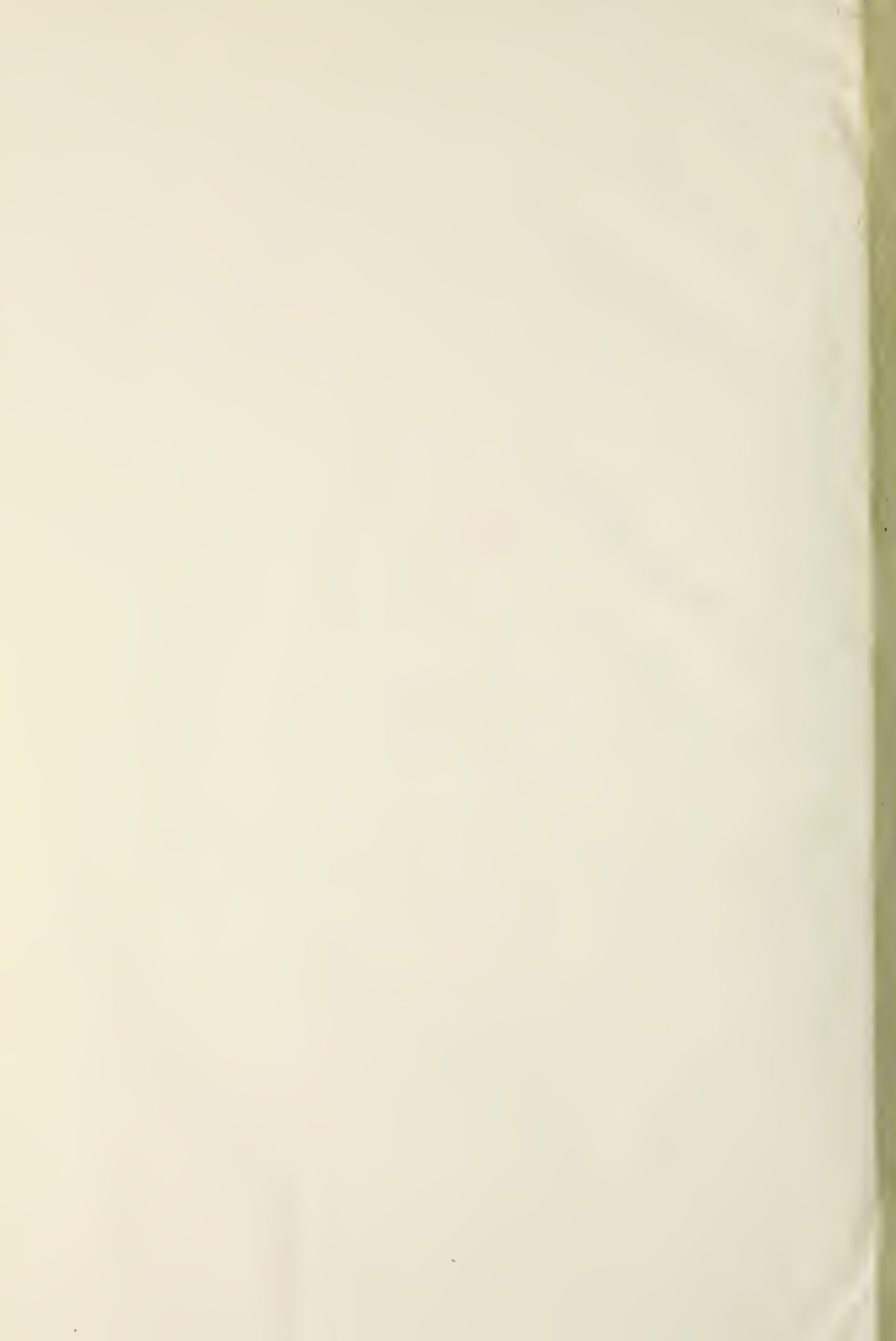
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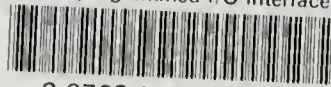
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